

MODEL NAME : *QLM00*
 PCB NO : *LA-7841P (DA*****)*
 BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Chief River)

Ivy Bridge ULV(BGA1023) + Panther Point

DISCRETE VGA N13P-GV(optimus)

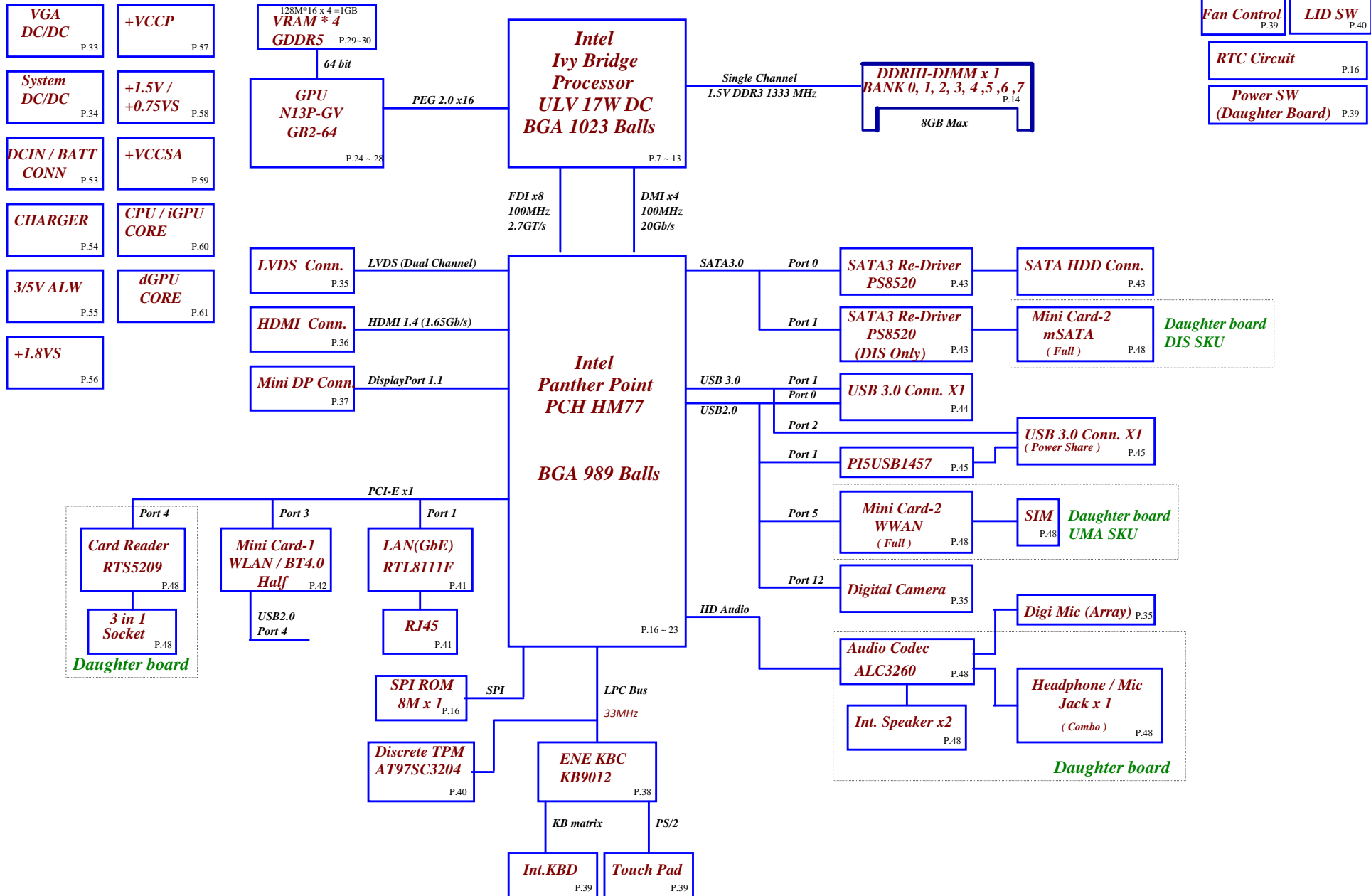
2012-01-19

Rev: 1.0 (X04)

@ : Nopop Component
 CONN@ : Connector Component
 DIS@ : pop when DIS configuration
 UMA@ : pop when UMA configuration

MB Type	BOM P/N	
TPM	4319EJ31L01	
TCM	4319EJ31L02	2@ 4@
TPM DIS/ TCM DIS		2@ 3@

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Project Code : QLM00
File Name : LA-7841P

LS-7841P POWER BUTTON BOARD
LS-7842P LED INDICATE BOARD
LS-7843P BATTERY INDICATED BOARD
LS-7844P I/O BOARD



Wire
6 pin



Wire

Camera

LCD Panel

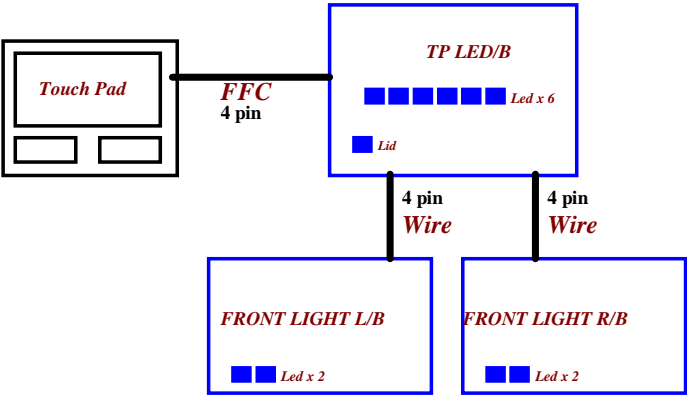
FFC

IO/B

Wire

HDD

FFC



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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDPA	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

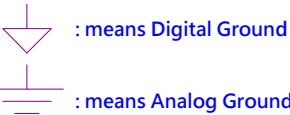
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

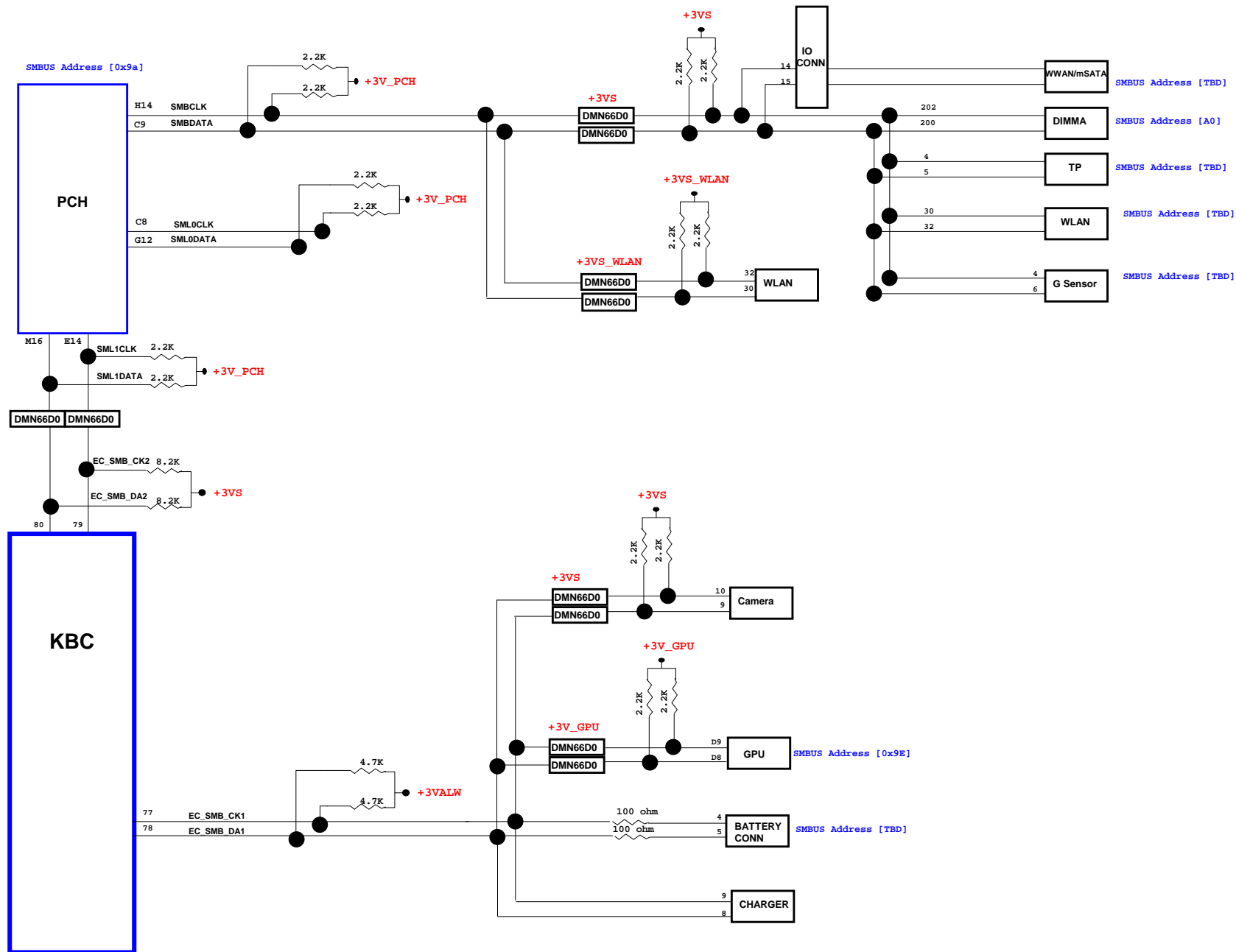
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

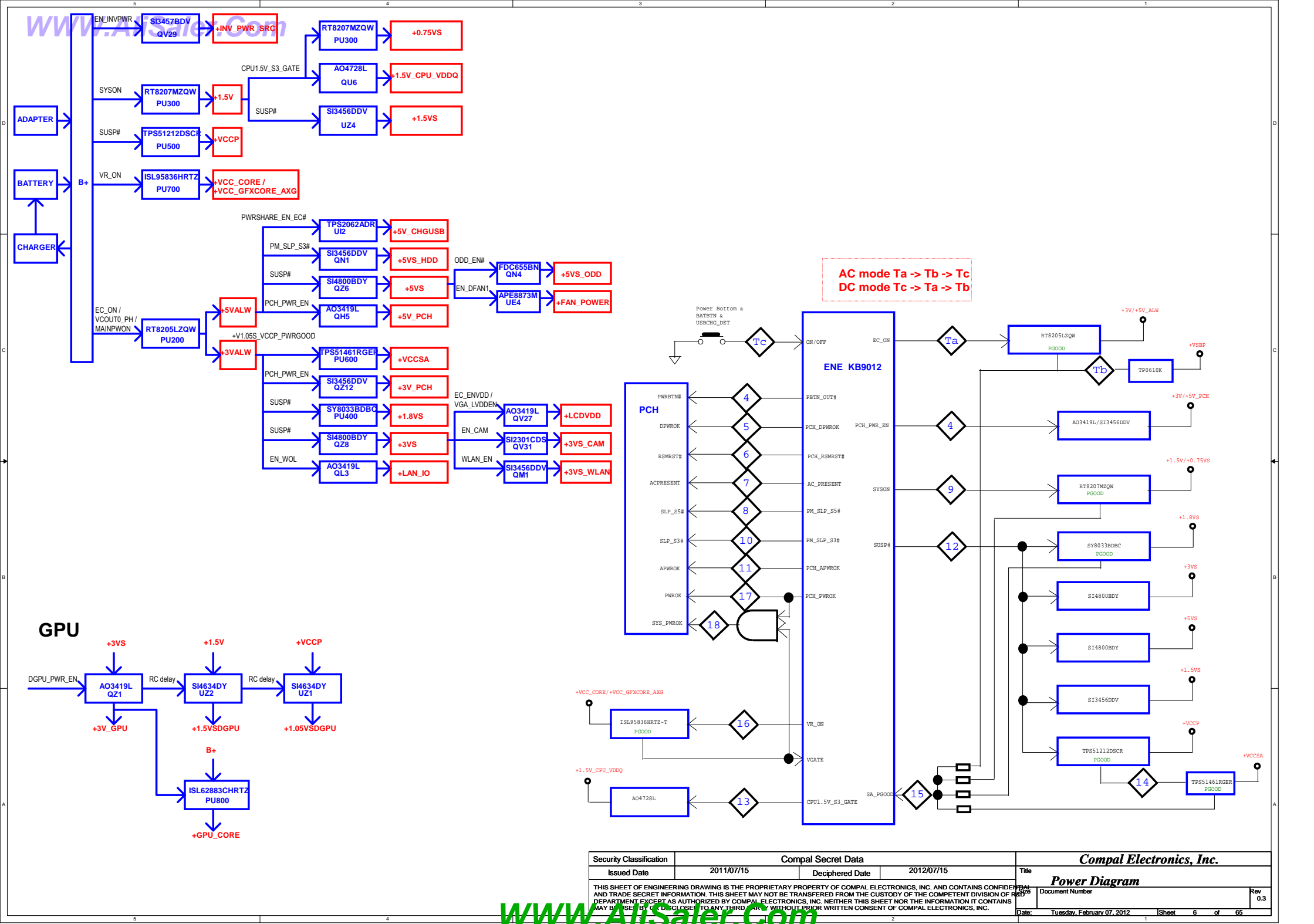
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

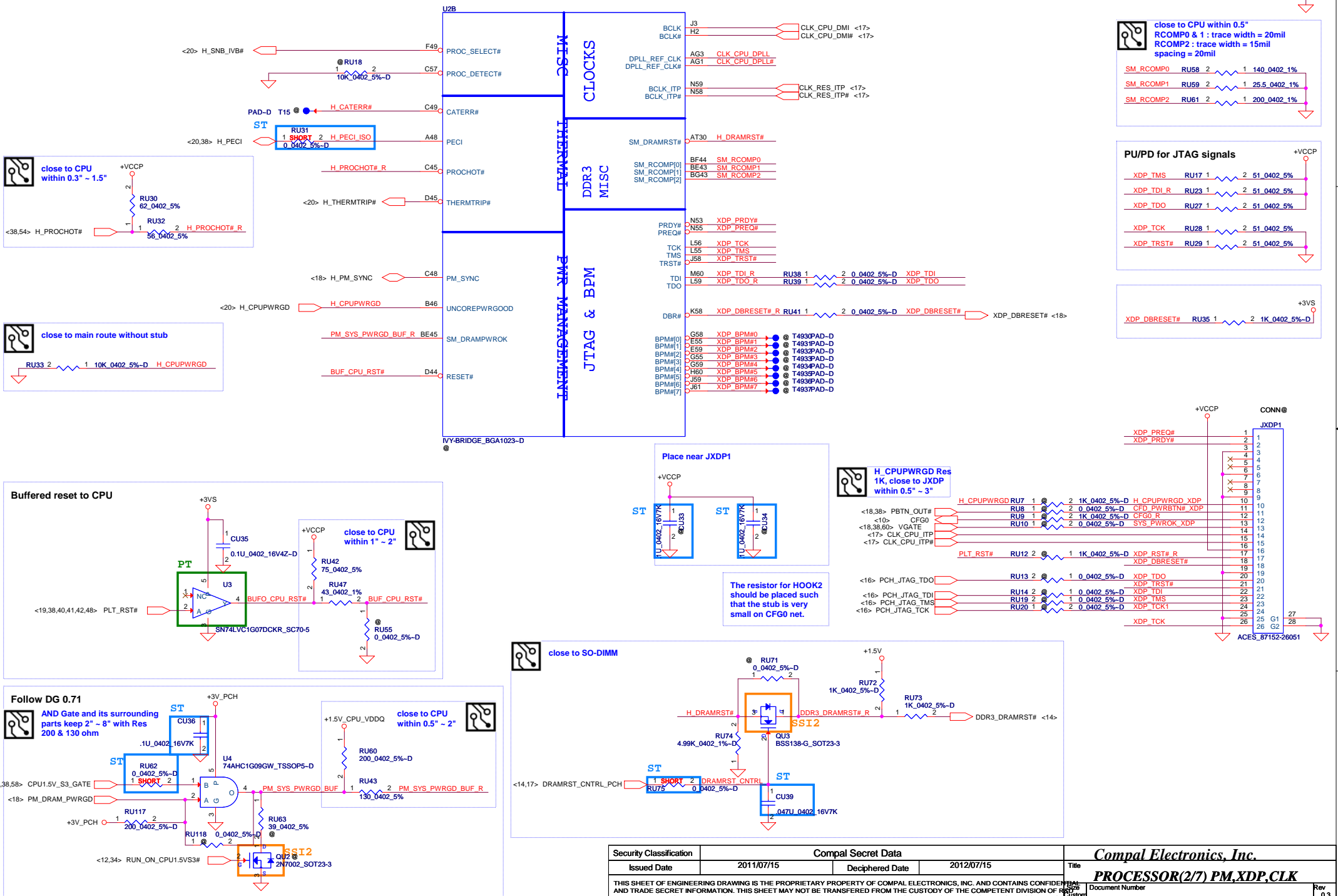
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

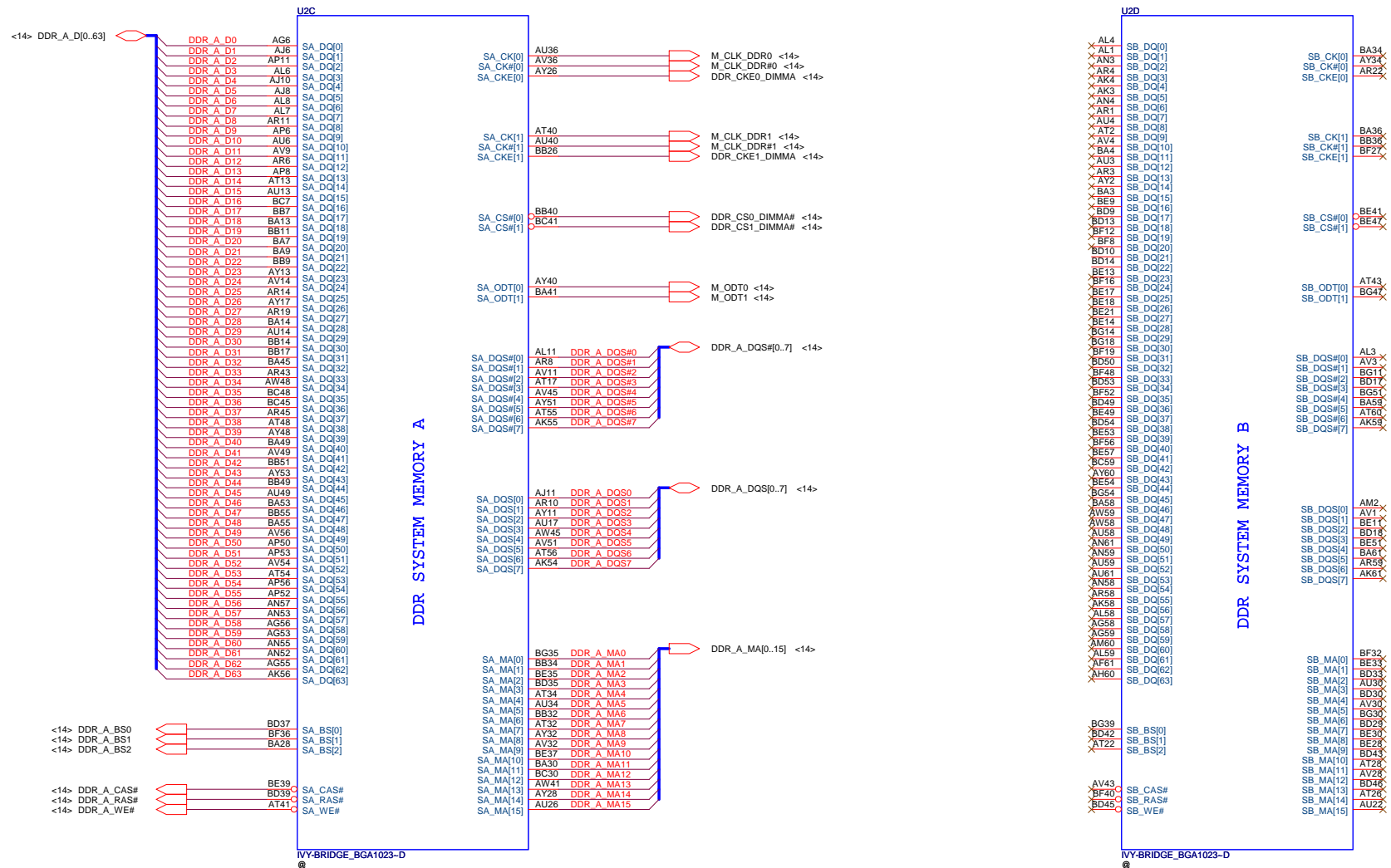
Symbol Note :

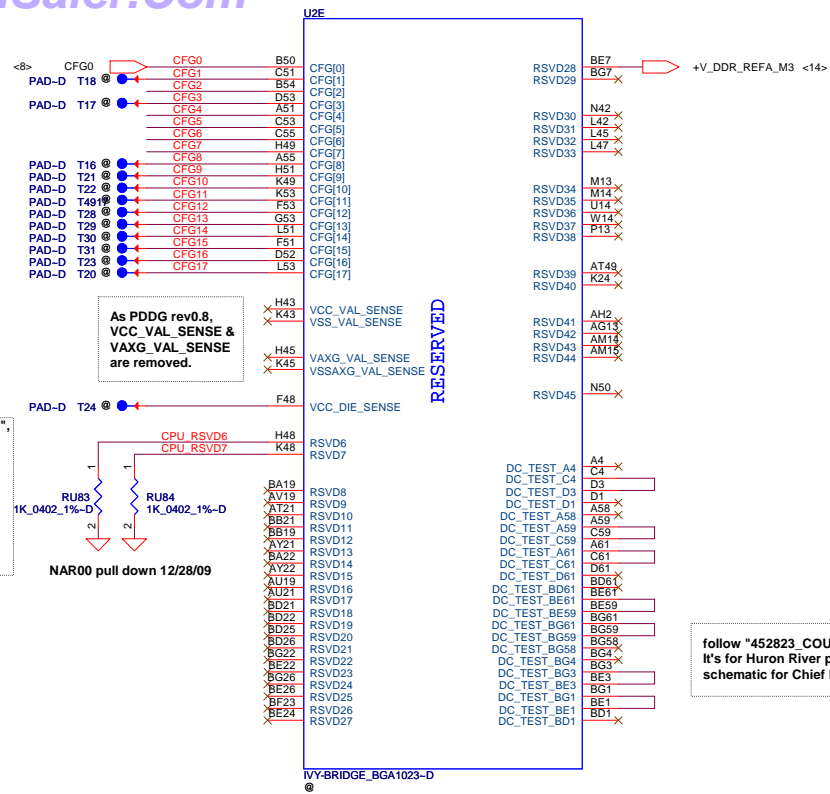




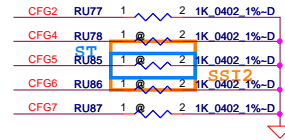








CFG Straps for Processor



		1 (Default value)	0
PCI Express* Static x16 Lane Numbering Reversal	CFG2	Normal operation (match socket pin map)	Lane numbers reversed
PCI Express* Static x4 Lane Numbering Reversal	CFG3	Normal operation (match socket pin map)	Lane numbers reversed
eDP enable	CFG4	Disable	Enable
PEG DEFER TRAINING	CFG7	PEG Train immediately following RESETB de-assertion	PEG Wait for BIOS for training

PCI Express Bifurcation (x16 Lane)	CFG[6:5]	11	1 x16 PCI Express (Default value)
		10	2 x8 PCI Express
		01	reserved
		00	1 x8, 2 x4 PCI Express

follow "452823_COUGAR_CANYON(BGA1023)_Customer_Ready_Schematic". It's for Huron River platform, since can't find CPU Ivy bridge BGA1023 schematic for Chief River at this moment.

+VCC_CORE decoupling
Cap. in Page 62.

+VCCP decoupling
Cap. in Page 62.

+VCCP
8.5A

+VCC_CORE

33A

ULV 17W, Max Current
in Turbo Mode or HFM

U2F

CORE SUPPLY

PEG IO AND DDR IO

QUIET
RAILS

SVZD

SENSE LINES

IYV-BRIDGE_BGA1023-D
①

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

VCCIO50 W16
VCCIO51 W17
1 CU40
2 1U_0402_6.3V6K-D

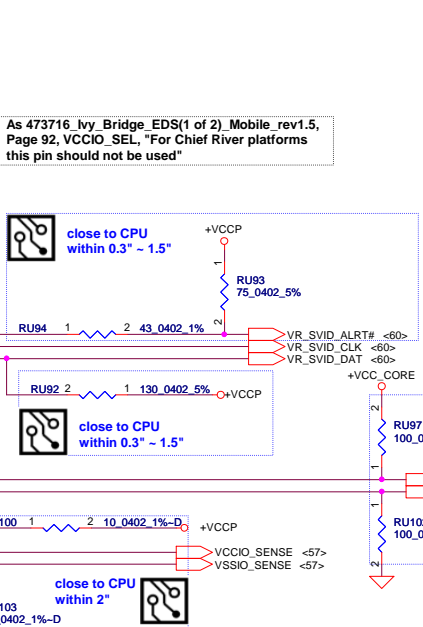
VCCIO_SEL BC22 T25 PAD-D
As 473716 Ivy Bridge EDS(1 of 2) Mobile_rev1.5,
Page 92, VCCIO_SEL, "For Chief River platforms
this pin should not be used"

VCCPQE[1] AM25
VCCPQE[2] AN22
1 CU94
2 1U_0402_6.3V6K-D

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43
VIDSOUT C44

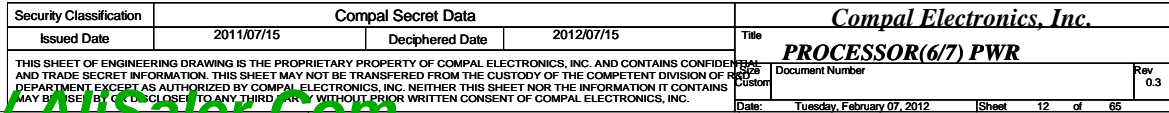
VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R

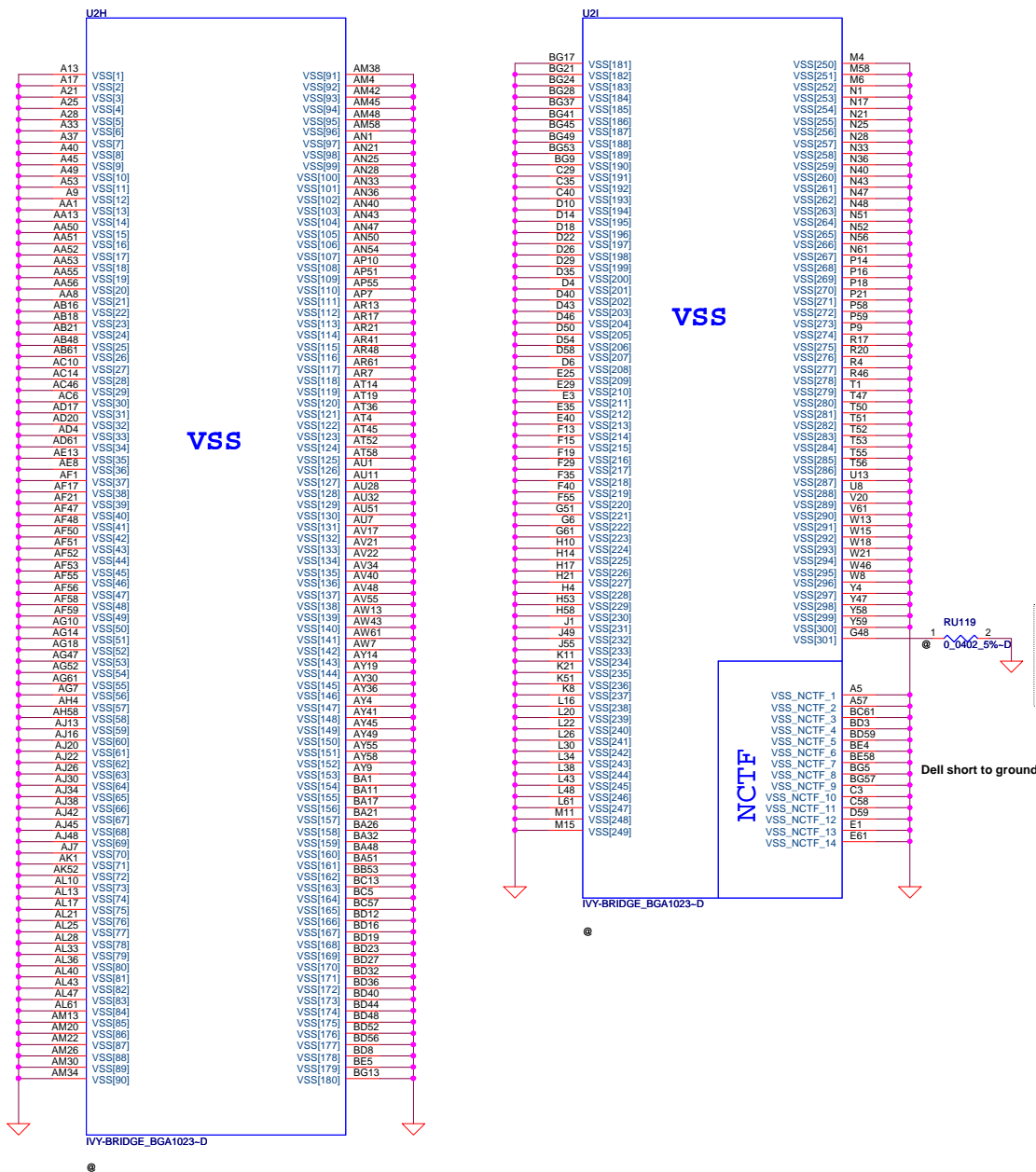
VCCIO_SENSE AN16 VCCIO SENSE_R
VSS_SENSE_VCCIO AN17 VSS SENSE VCCIO
1 RU100 2 10_0402_1%-D
1 RU103 2 10_0402_1%-D



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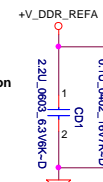
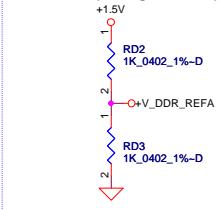
Compal Electronics, Inc.	
Title	PROCESSOR(5/7) PWR,BYPASS
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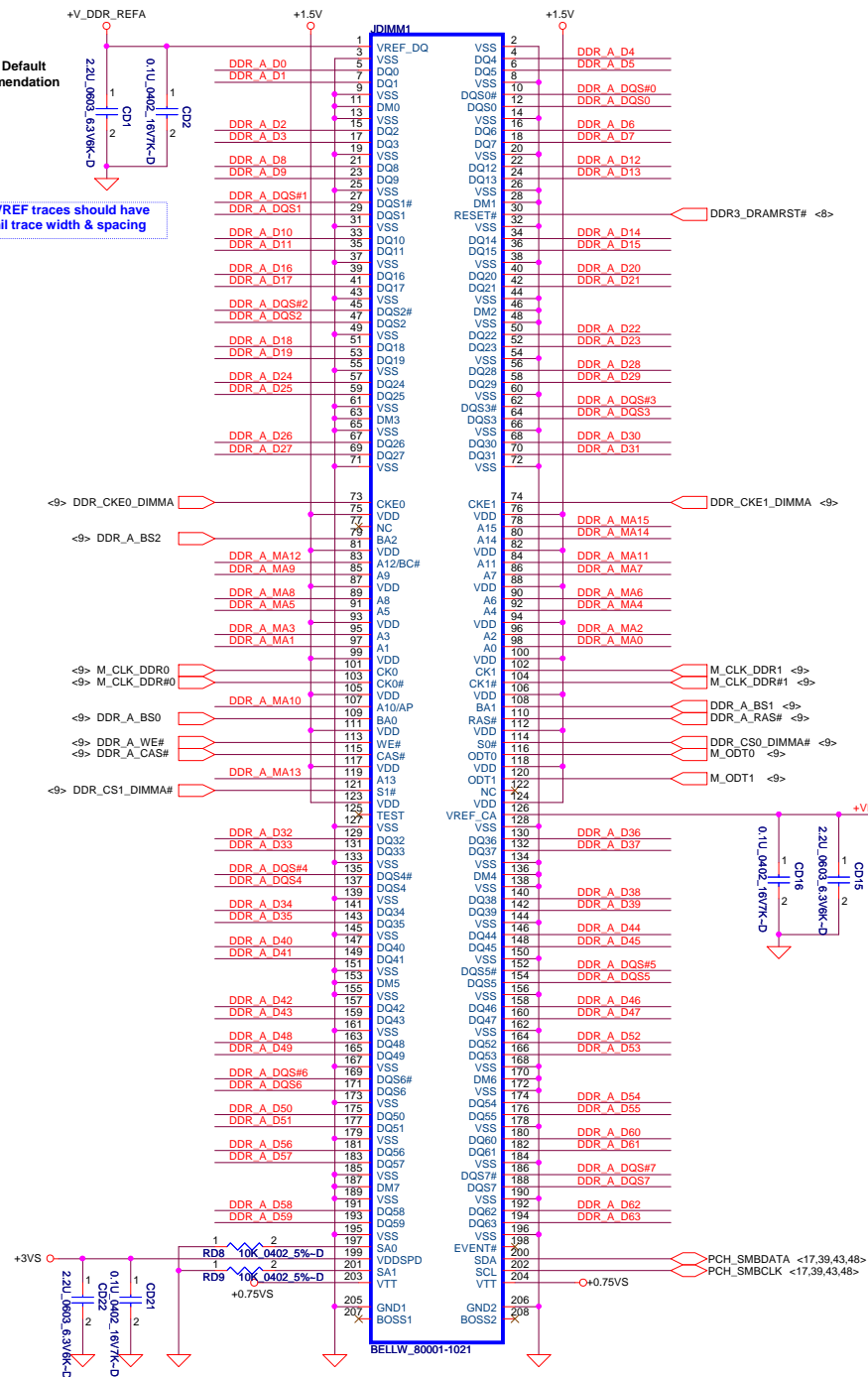
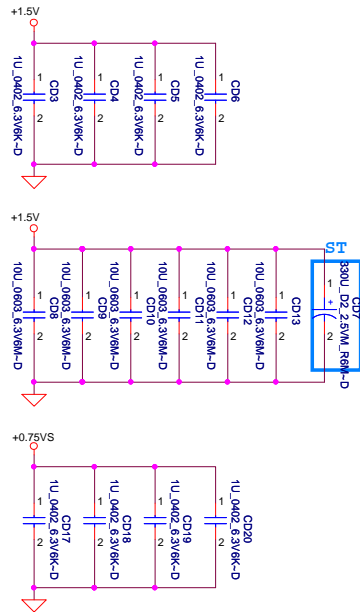
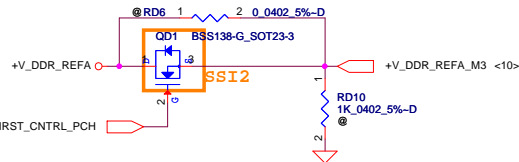


follow "458544_CR_PDDG_rev.0.8", section "2.2.1", Intel recommends providing accessibility to the pins F48 & G48 for debug purpose. The pins should be via through to the backside of the board to allow backside probing with no connection to other rails/components on the platform.

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**All VREF traces should have
20mil trace width & spacing**

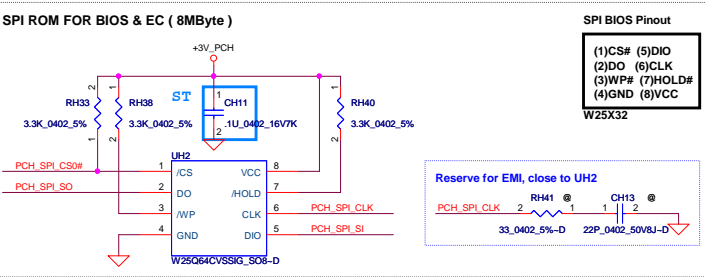
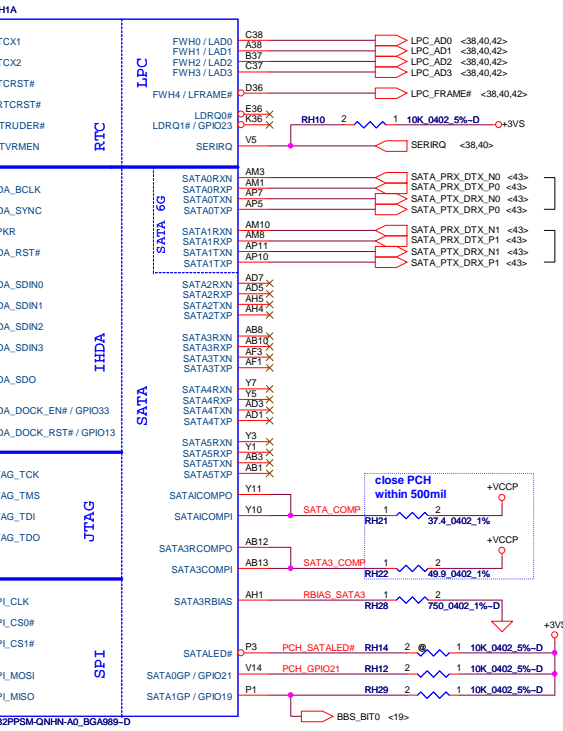
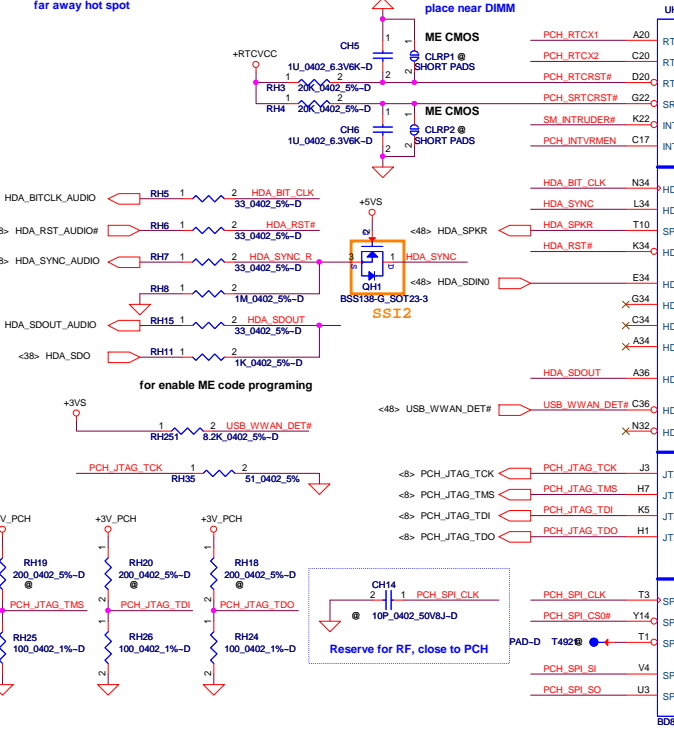
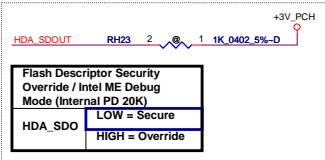
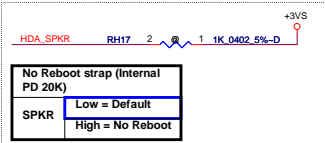
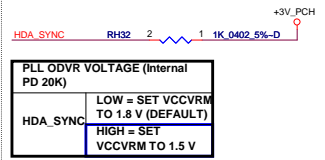
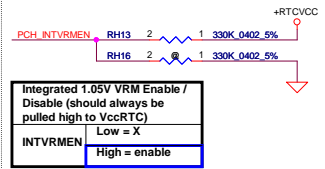
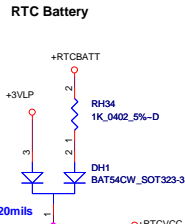
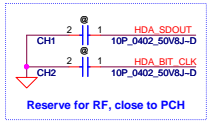
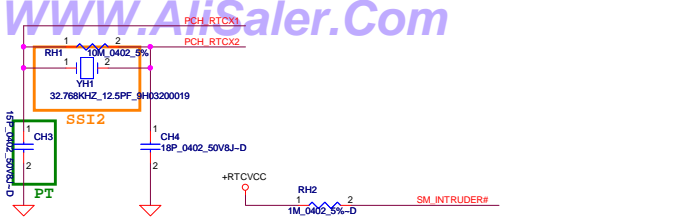


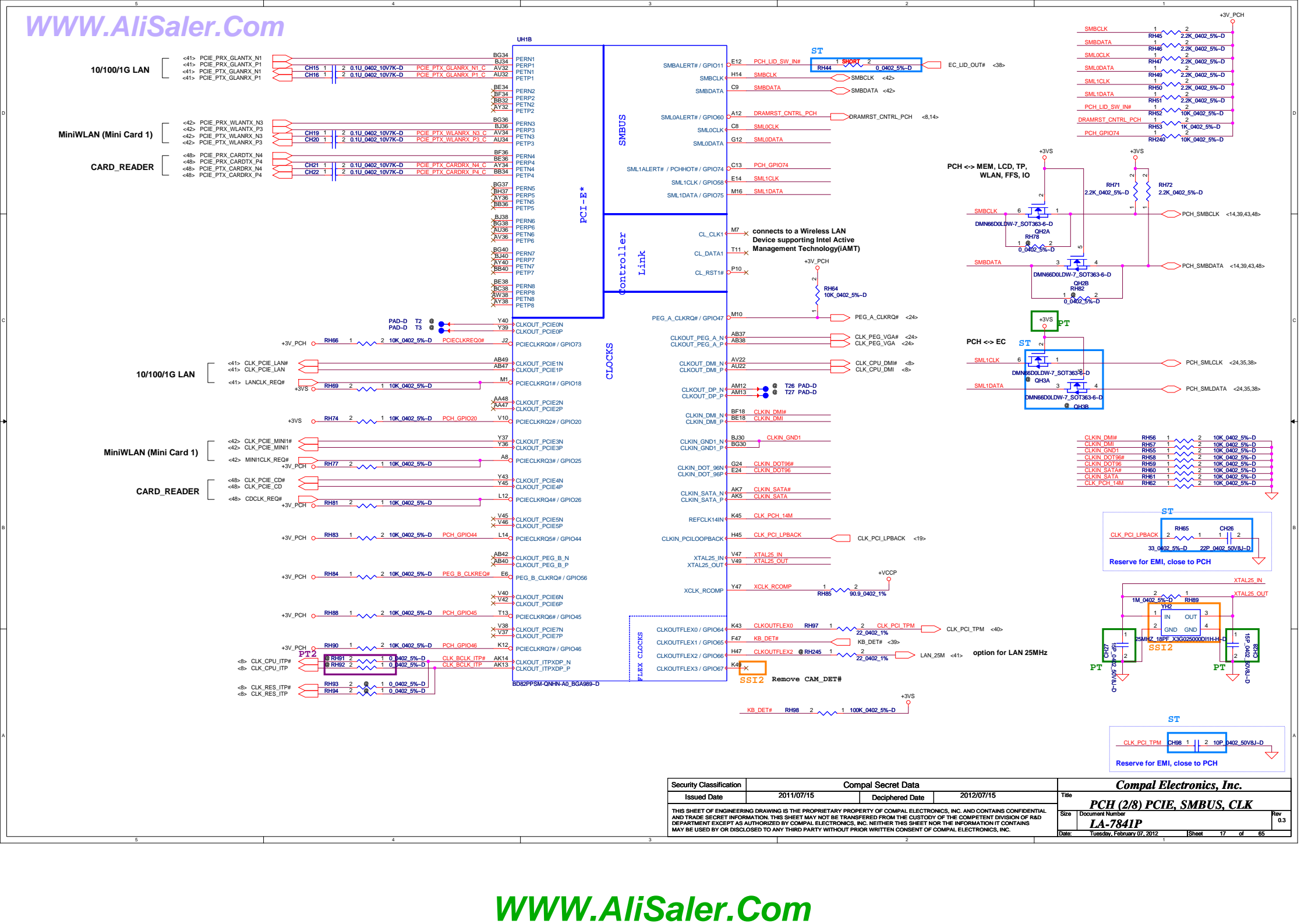
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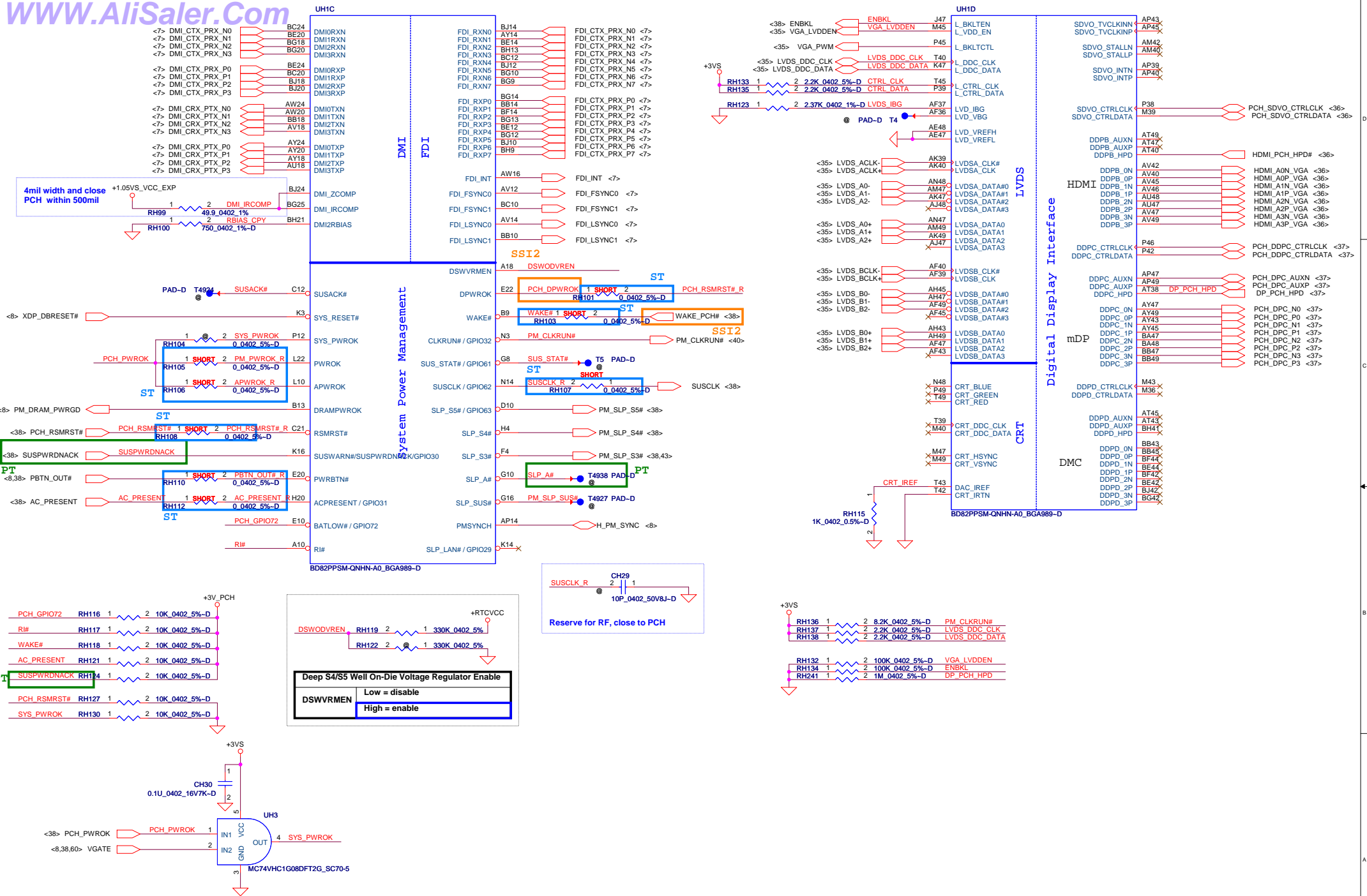
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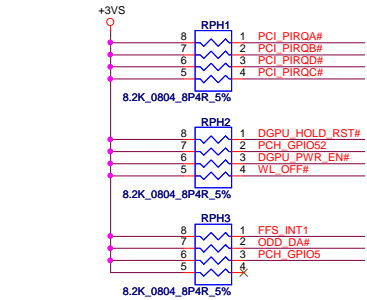
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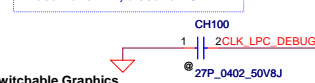
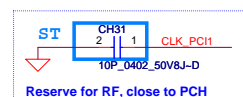
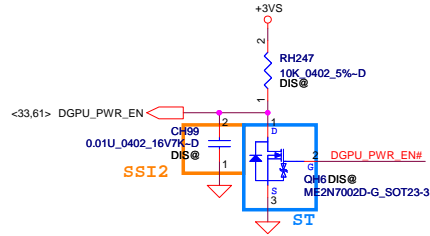
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Boot BIOS Strap (Both internal PU 20K)		
BIT 1	BIT 0	Boot BIOS Location
GNT1#	SATA1GP	
0	0	LPC
0	1	Reserved
1	0	PCI(non-mobile)
1	1	SPi

A16 Top-Block Swap Override (Internal PU 20K)	
GNT3#	
Low = swap enabled	
High = Default	

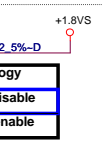
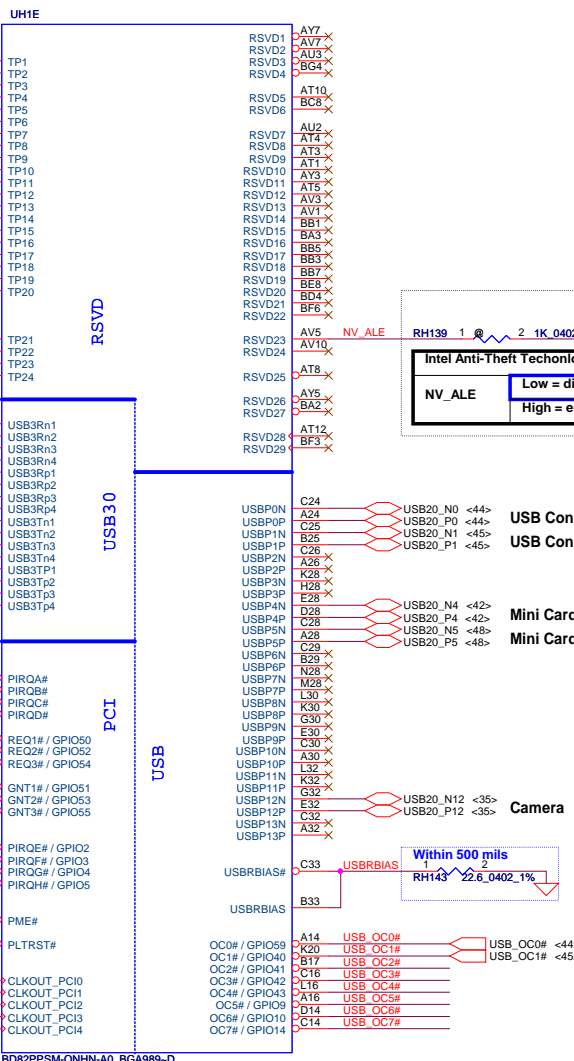
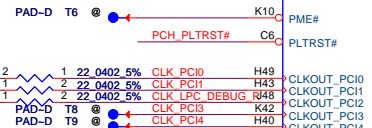


USB Conn 1
USB Conn 2 (Power Share)



Signal	GPIO	Type	DuringReset	After Reset	Usage	Description
DGPU_PWR_EN#	GPIO54	Output	High	High	Must have	Driven by Switchable Graphics Driver to turn on/off the discrete graphics power. 0 = dGPU power switch turned on 1 = Power switch turned off
DGPU_PWROK	GPIO17	Input	-	-	Must have	Driven by dGPU VR to indicate the power status to PCH. Used to enable clocks to dGPU. 0 = dGPU power is not stable. Keep clock disabled & reset asserted. 1 = dGPU power is stable. Clock can be enabled; reset can be deasserted. If DGPU_PRST# is 1, in-order to get regular discrete GFX cards working, program DGPU_PWROK as GPO and assert a high value (1) on the pin.
DGPU_HOLD_RST#	GPIO50	Output	Low	Low	Must have	Discrete Graphics Enable signal. Controlled by Switchable Graphics Driver and driven by PCH GPIO. Used to gate with Platform Reset to enable the Reset for dGPU. 0 = Keep dGPU in reset. 1 = Reset is released. This action taken 100 ms after DGPU_PWROK to ensure clock is stable.

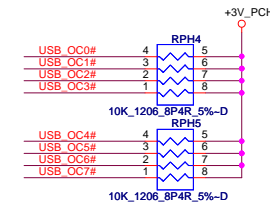
REQ[1:3]# & GNT[1:3]# are used as GPIO on Mobile
GNT[1:3]# have internal weak PU, and disable after PLTRST# deassert



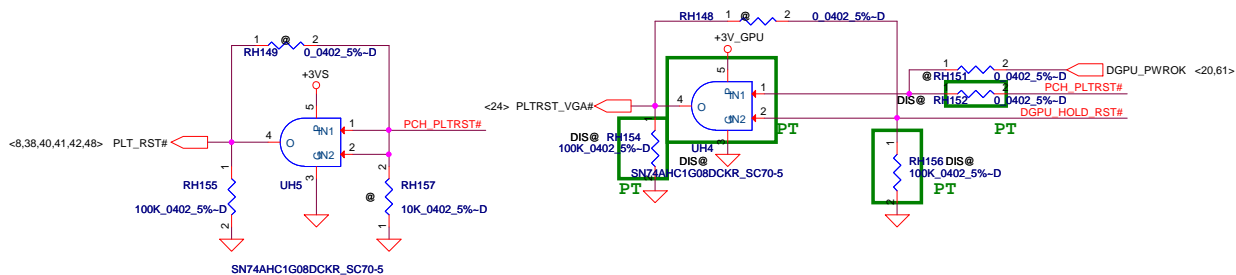
USB Conn 1
USB Conn 2 (Power Share)

Mini Card(WLAN)
Mini Card(WWAN)

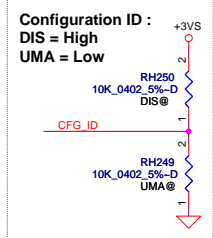
Camera



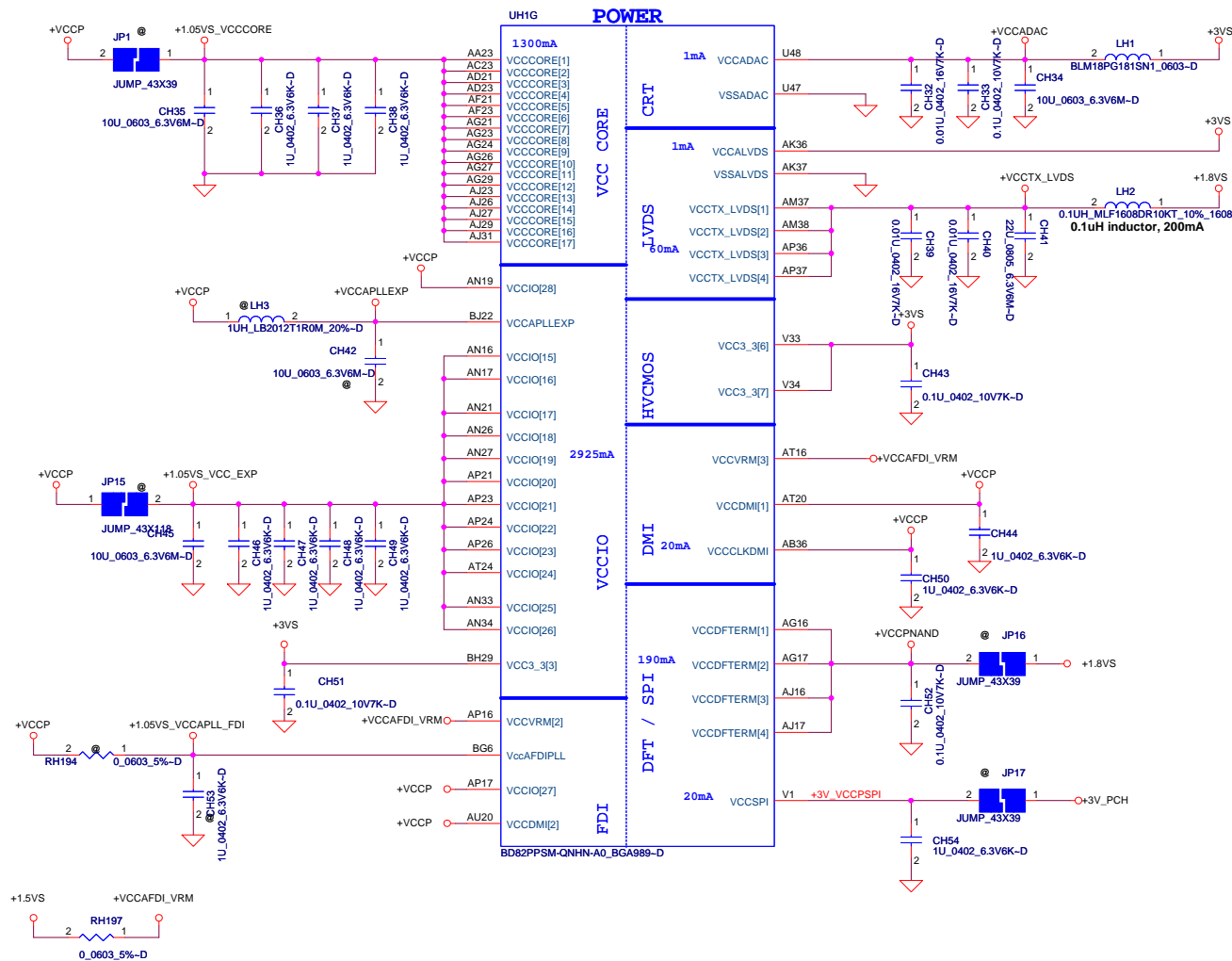
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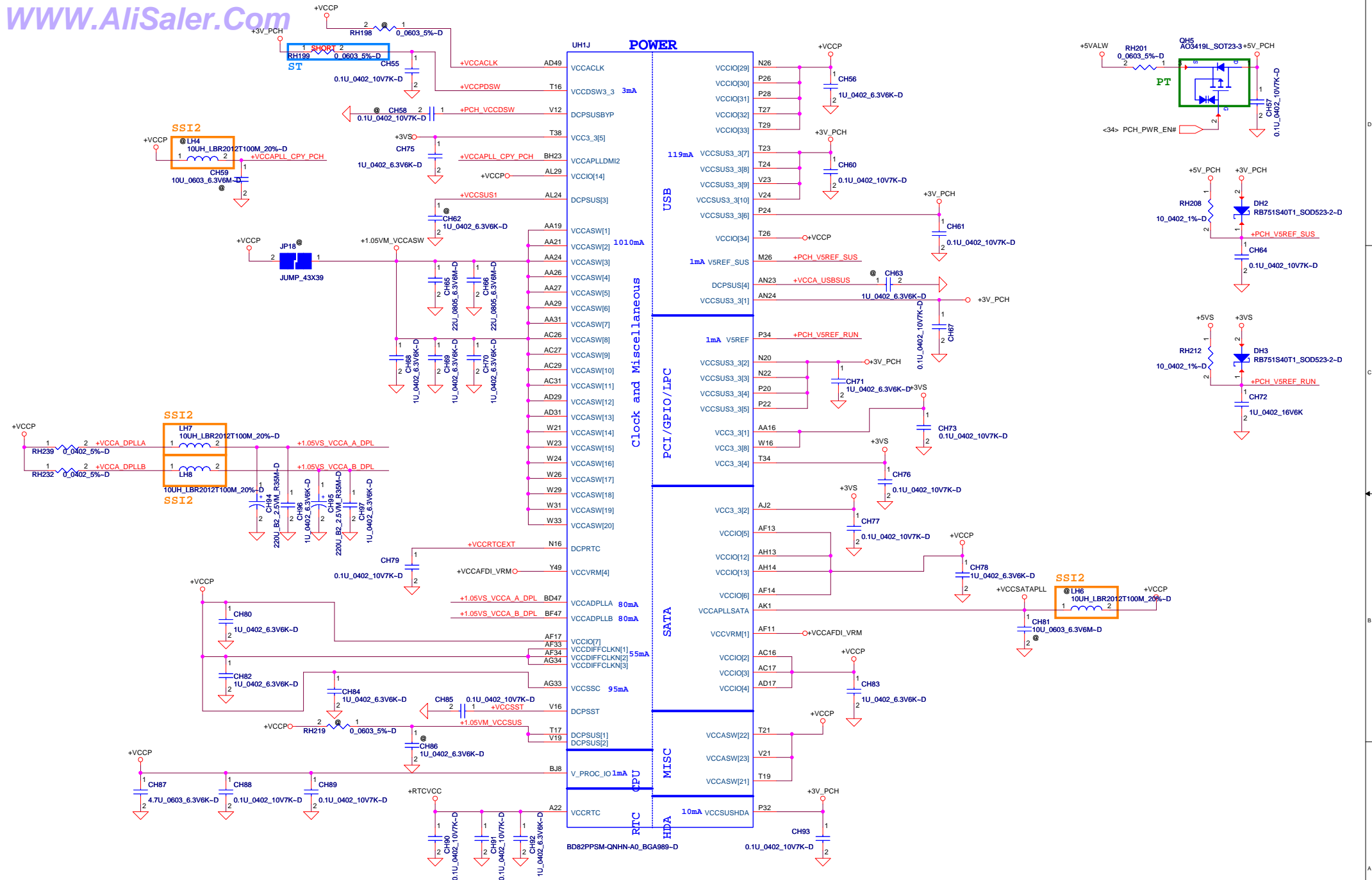
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PCH Power Rail Table		
Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



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				Document Number		LA-7841P	
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				Sheet		22 of 65	
				Rev		0.3	

UH1H		
H5	VSS[0]	
AA17	VSS[1]	AK38
AA2	VSS[2]	AK4
AA3	VSS[3]	AK42
AA33	VSS[4]	AK45
AA34	VSS[5]	AK8
AB11	VSS[6]	AL16
AB14	VSS[7]	AL17
AB39	VSS[8]	AL19
AB4	VSS[9]	AL2
AB43	VSS[10]	AL21
AB5	VSS[11]	AL23
AB7	VSS[12]	AL26
AC19	VSS[13]	AL27
AC2	VSS[14]	AL31
AC21	VSS[15]	AL33
AC24	VSS[16]	AL34
AC33	VSS[17]	AL48
AC34	VSS[18]	AM11
AC48	VSS[19]	AM14
AD10	VSS[20]	AM36
AD11	VSS[21]	AM39
AD12	VSS[22]	AM100
AD13	VSS[23]	AM101
AD19	VSS[24]	AM102
AD24	VSS[25]	AM103
AD26	VSS[26]	AM104
AD27	VSS[27]	AM105
AD33	VSS[28]	AM106
AD34	VSS[29]	AM107
AD36	VSS[30]	AM108
AD37	VSS[31]	AM109
AD38	VSS[32]	AM110
AD39	VSS[33]	AM111
AD4	VSS[34]	AM112
AD40	VSS[35]	AM113
AD42	VSS[36]	AM114
AD43	VSS[37]	AM115
AD45	VSS[38]	AM116
AD46	VSS[39]	AM117
AD8	VSS[40]	AM118
AE2	VSS[41]	AM119
AE3	VSS[42]	AM120
AF10	VSS[43]	AM121
AF12	VSS[44]	AM122
AD14	VSS[45]	AM123
AD16	VSS[46]	AM124
AF16	VSS[47]	AM125
AF19	VSS[48]	AM126
AF24	VSS[49]	AM127
AF26	VSS[50]	AM128
AF27	VSS[51]	AM129
AF29	VSS[52]	AM130
AF31	VSS[53]	AM131
AF38	VSS[54]	AM132
AF4	VSS[55]	AM133
AF42	VSS[56]	AM134
AF46	VSS[57]	AM135
AF5	VSS[58]	AM136
AF7	VSS[59]	AM137
AF8	VSS[60]	AM138
AG19	VSS[61]	AM139
AG2	VSS[62]	AM140
AG31	VSS[63]	AM141
AG48	VSS[64]	AM142
AH11	VSS[65]	AM143
AH3	VSS[66]	AM144
AH36	VSS[67]	AM145
AH39	VSS[68]	AM146
AH40	VSS[69]	AM147
AH42	VSS[70]	AM148
AH46	VSS[71]	AM149
AH7	VSS[72]	AM150
AJ19	VSS[73]	AM151
AJ21	VSS[74]	AM152
AJ24	VSS[75]	AM153
AJ33	VSS[76]	AM154
AJ34	VSS[77]	AM155
AK12	VSS[78]	AM156
AK3	VSS[79]	AM157

BD82PPSM-QNH-N-A0_BGA989-D

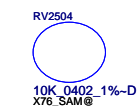
UH1		
AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B35	VSS[169]	L28
B39	VSS[170]	L36
B7	VSS[171]	L48
F45	VSS[172]	M12
B812	VSS[173]	M16
BB16	VSS[174]	M18
BB20	VSS[175]	M22
BB22	VSS[176]	M24
BB24	VSS[177]	M30
BB28	VSS[178]	M32
BB30	VSS[179]	M34
BB38	VSS[180]	M38
B84	VSS[181]	M4
BB46	VSS[182]	M42
BC14	VSS[183]	M46
BC18	VSS[184]	M8
BC2	VSS[185]	N18
BC22	VSS[186]	P30
BC26	VSS[187]	N47
BC32	VSS[188]	P11
BC34	VSS[189]	P18
BC36	VSS[190]	T33
BC40	VSS[191]	VSS[290]
BC42	VSS[192]	VSS[291]
BC48	VSS[193]	VSS[292]
BC11	VSS[194]	VSS[293]
BD5	VSS[195]	VSS[294]
BE22	VSS[196]	VSS[295]
BE26	VSS[197]	VSS[296]
BF10	VSS[198]	VSS[297]
BF12	VSS[199]	VSS[298]
BF16	VSS[200]	VSS[299]
BF20	VSS[201]	VSS[300]
BF22	VSS[202]	VSS[301]
BF24	VSS[203]	VSS[302]
BF26	VSS[204]	VSS[303]
BF28	VSS[205]	VSS[304]
BD3	VSS[206]	VSS[305]
BF30	VSS[207]	VSS[306]
BF38	VSS[208]	VSS[307]
BF40	VSS[209]	VSS[308]
BF48	VSS[210]	VSS[309]
BG17	VSS[211]	VSS[310]
BG21	VSS[212]	VSS[311]
BG33	VSS[213]	VSS[312]
AT34	VSS[214]	VSS[313]
BG8	VSS[215]	VSS[314]
BH11	VSS[216]	VSS[315]
BH15	VSS[217]	VSS[316]
BH17	VSS[218]	VSS[317]
BH19	VSS[219]	VSS[318]
H10	VSS[220]	VSS[319]
BH27	VSS[221]	VSS[320]
BH31	VSS[222]	VSS[321]
BH33	VSS[223]	VSS[322]
BH35	VSS[224]	VSS[323]
BH39	VSS[225]	VSS[324]
BH43	VSS[226]	VSS[325]
BH7	VSS[227]	VSS[326]
D3	VSS[228]	VSS[327]
D12	VSS[229]	VSS[328]
D16	VSS[230]	VSS[329]
D18	VSS[231]	VSS[330]
D22	VSS[232]	VSS[331]
D24	VSS[233]	VSS[332]
D26	VSS[234]	VSS[333]
D30	VSS[235]	VSS[334]
D32	VSS[236]	VSS[335]
D34	VSS[237]	VSS[336]
D38	VSS[238]	VSS[337]
D42	VSS[239]	VSS[338]
D8	VSS[240]	VSS[339]
E18	VSS[241]	VSS[340]
E26	VSS[242]	VSS[341]
G18	VSS[243]	VSS[342]
G20	VSS[244]	VSS[343]
G26	VSS[245]	VSS[344]
G28	VSS[246]	VSS[345]
G36	VSS[247]	VSS[346]
G48	VSS[248]	VSS[347]
H12	VSS[249]	VSS[348]
H18	VSS[250]	VSS[349]
H22	VSS[251]	VSS[350]
H24	VSS[252]	VSS[351]
H26	VSS[253]	VSS[352]
H30	VSS[254]	
H34	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

BD82PPSM-QNH-N-A0_BGA989-D





PT



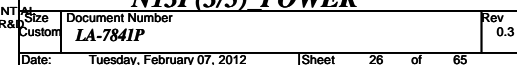
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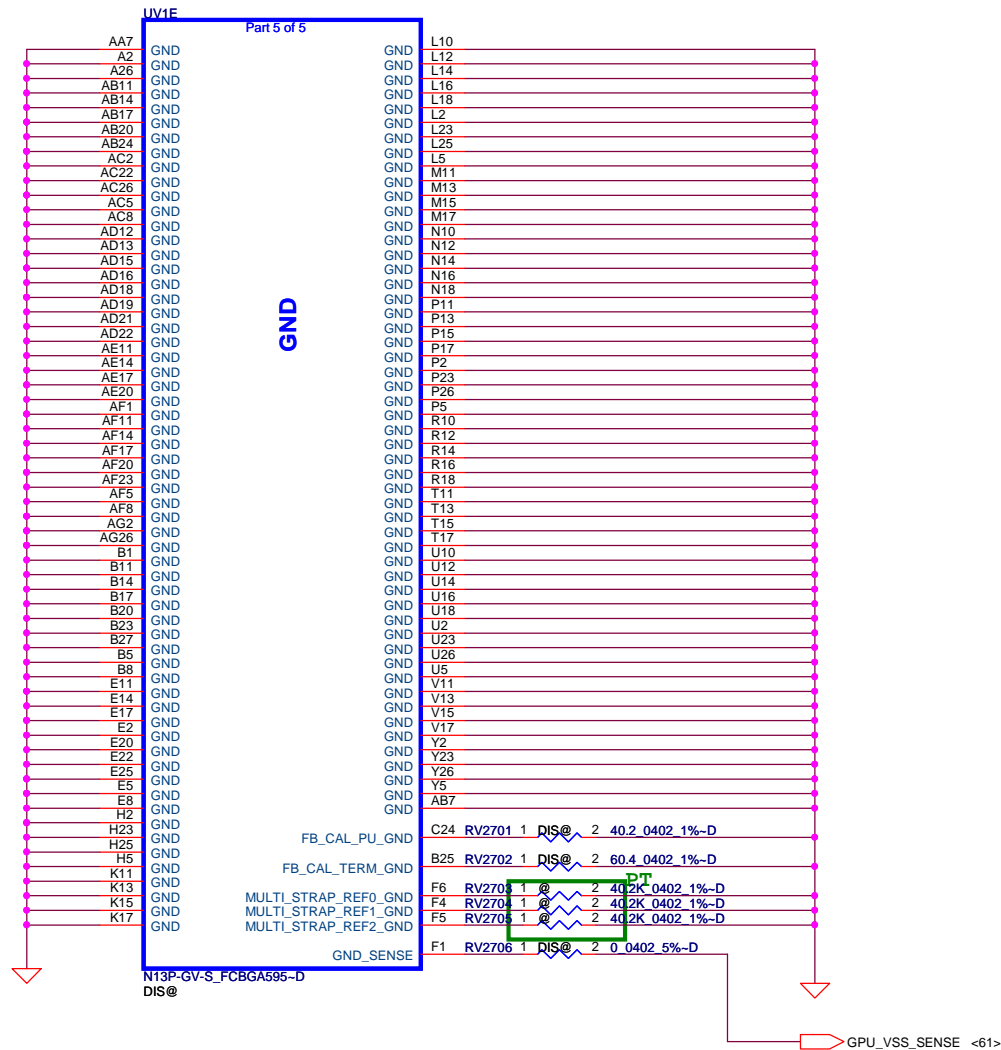
Binary Mode Straps

STRAP Pin Name

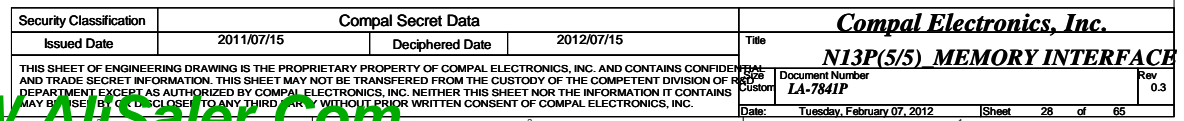
STRAP0	RAM_CFG[0]	10K Ohm	For Hynix Pull-down 10K ohm to GND, Samsung pull-high 10K ohm to 3.3V
STRAP1	RAM_CFG[1]	10K Ohm	Pull-down 10K ohm to GND
STRAP2	RAM_CFG[2]	10K Ohm	Pull-up 10K ohm to +3V_GPU
STRAP3	RAM_CFG[3]	10K Ohm	Pull-down 10K ohm to GND
STRAP4	PCIE_MAX_SPEED	10K Ohm	Pull-down 10K ohm to GND
ROM_SCLK	SMB_ALT_ADDR	10K Ohm	Pull-down 10K ohm to GND
ROM_SI	SUB_VENDOR	10K Ohm	Pull-down 10K ohm to GND
ROM_SO	VGA_DEVICE	10K Ohm	Pull-down 10K ohm to GND

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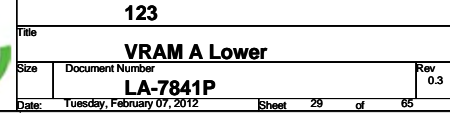
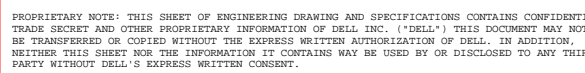
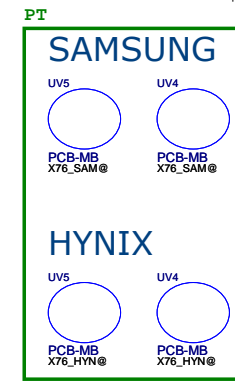
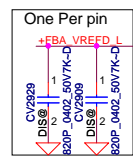
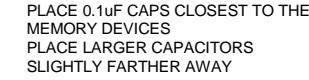
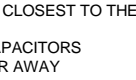
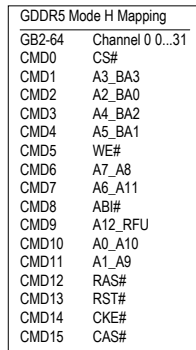




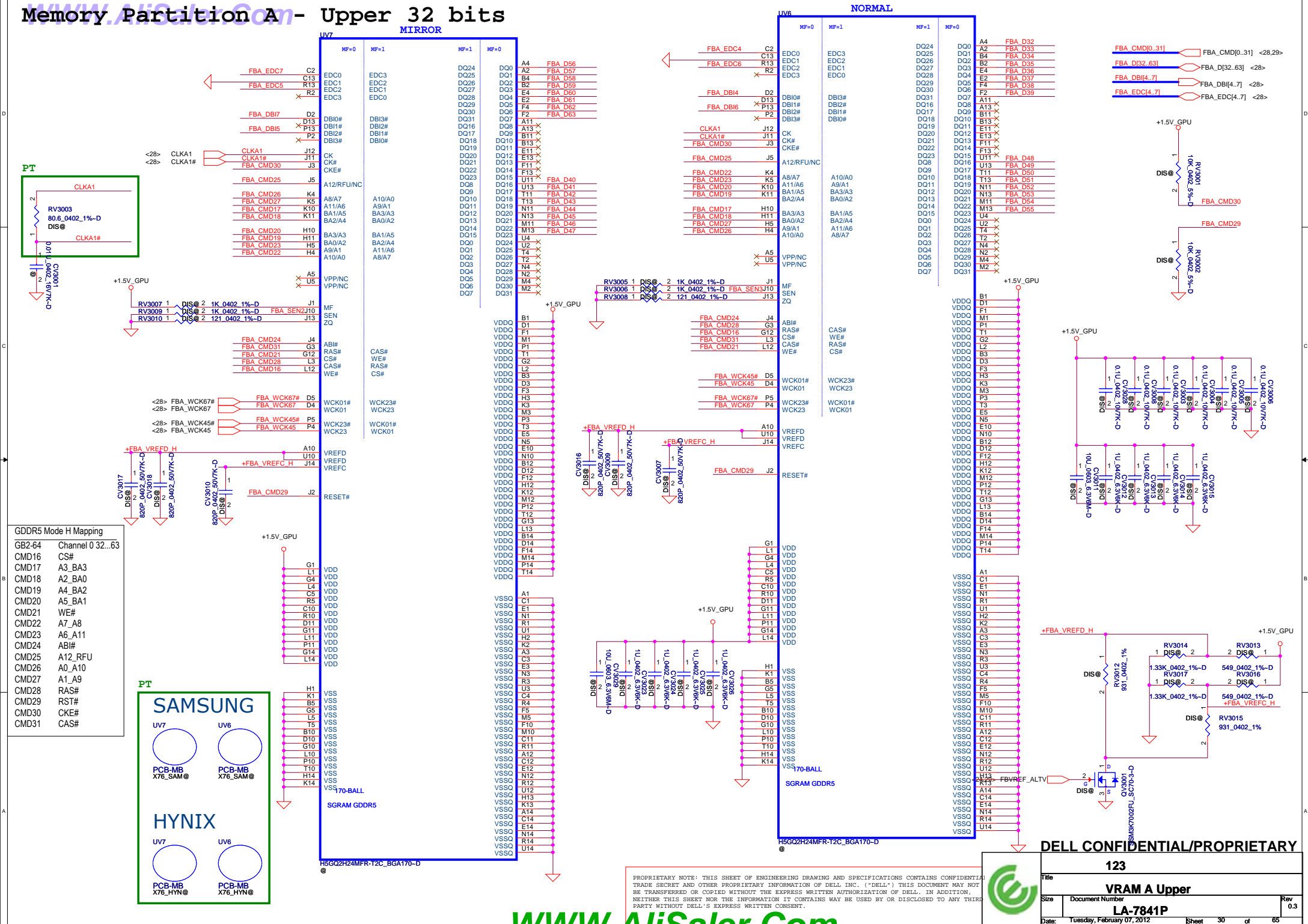
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DATA Bus		
Address	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS#	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



Memory Partition A - Upper 32 bits



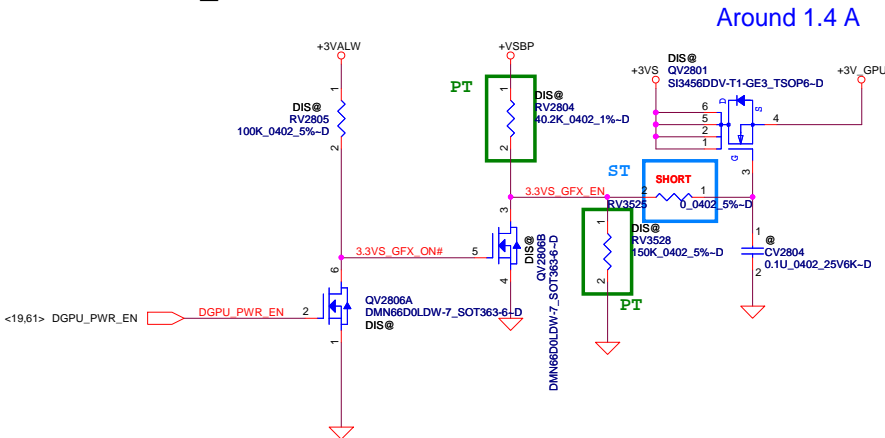
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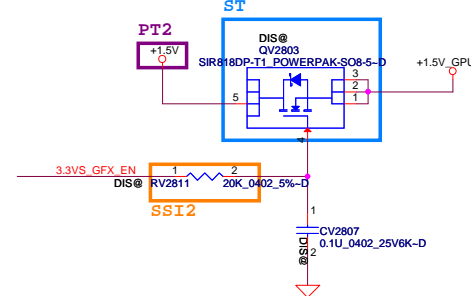
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				Date: Tuesday, February 07, 2012	Sheet 32 of 65

+3VS to +3V_GPU



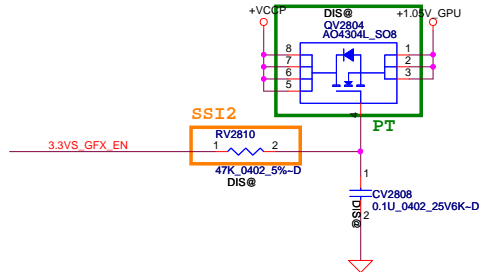
+1.5VS to +1.5V_GPU

Around 4.5 A+1.44A X 4pcs VRAM=10.26A

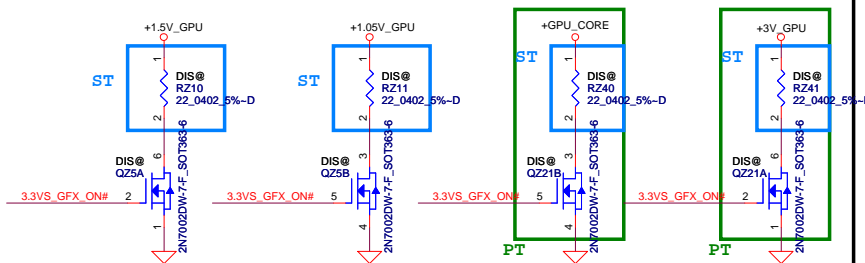


+1.05VS to +1.05V_GPU

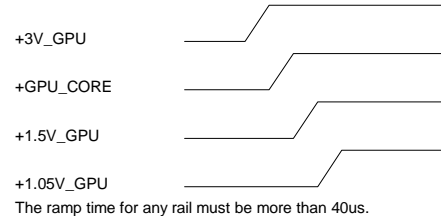
Around 3 A



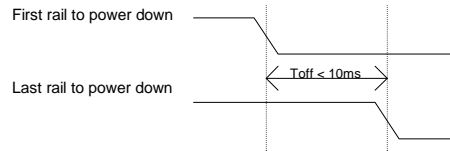
GPU Power Discharge Path



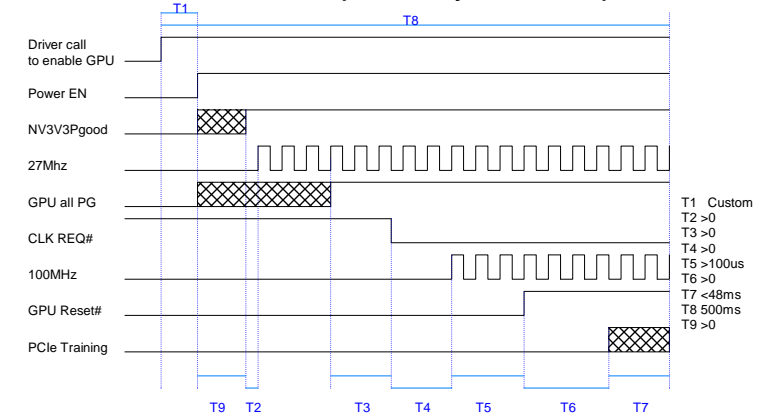
GPU Power Up Power Rail Sequence



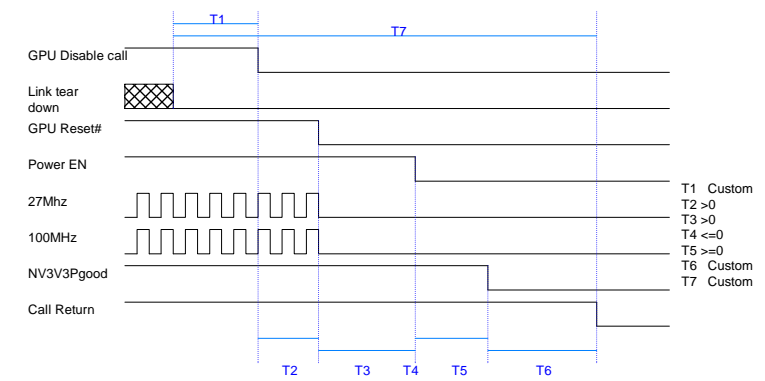
GPU Power Down Sequence



GPU Power Up Sub-system Sequence

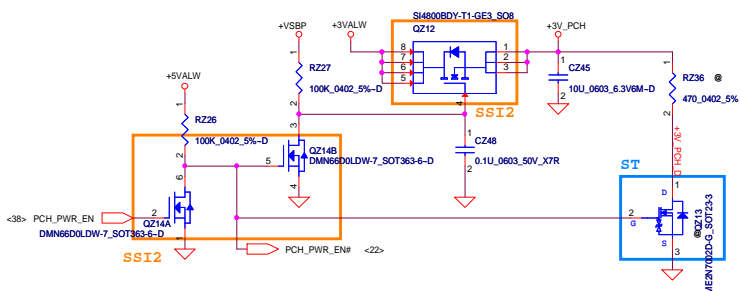


GPU Power Down Sub-system Sequence

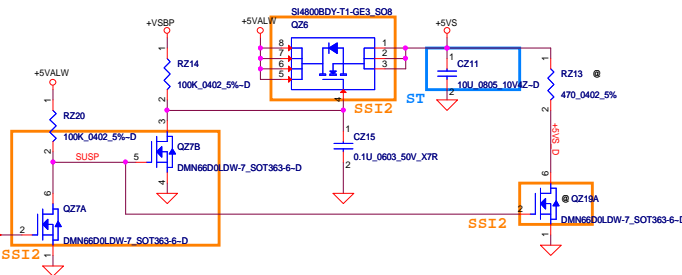


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Date: Tuesday, February 07, 2012				Rev 0.3

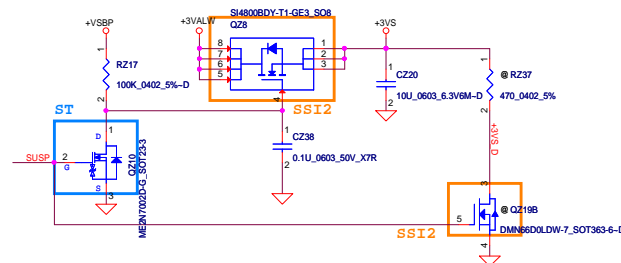
+3VALW to +3V_PCH



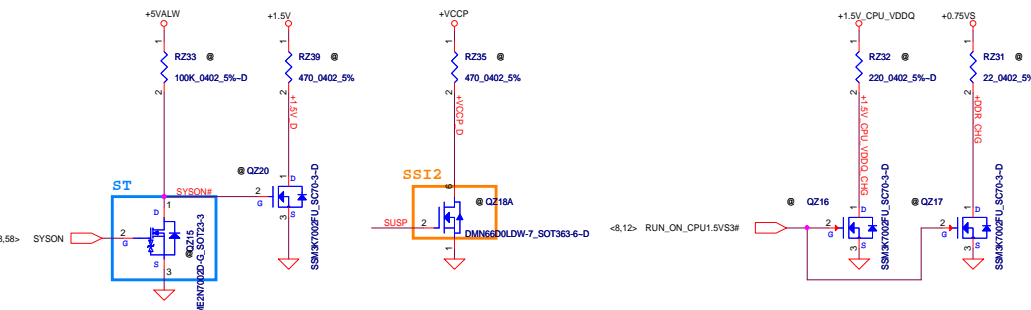
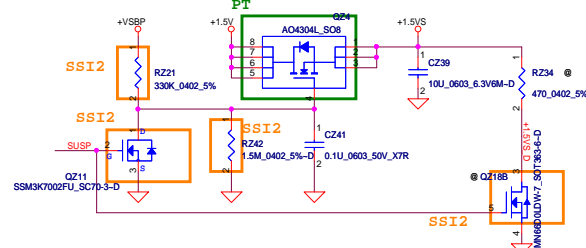
+5VALW to +5VS



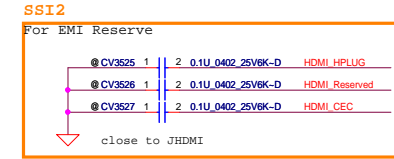
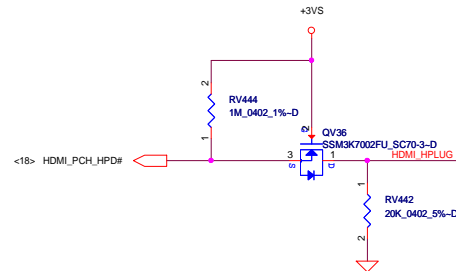
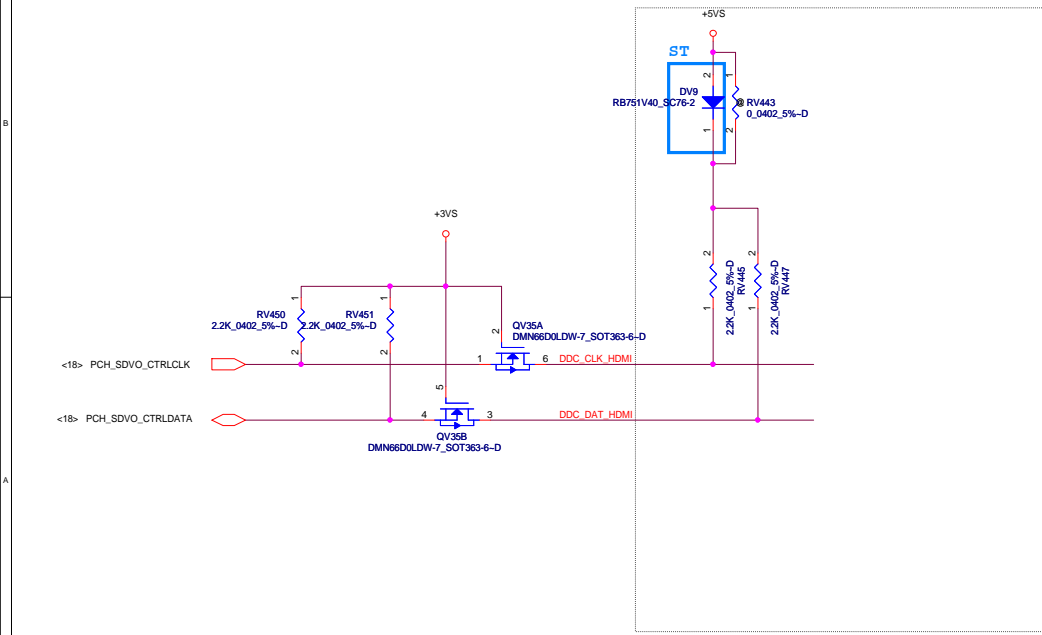
+3VALW to +3VS



+1.5V To +1.5VS

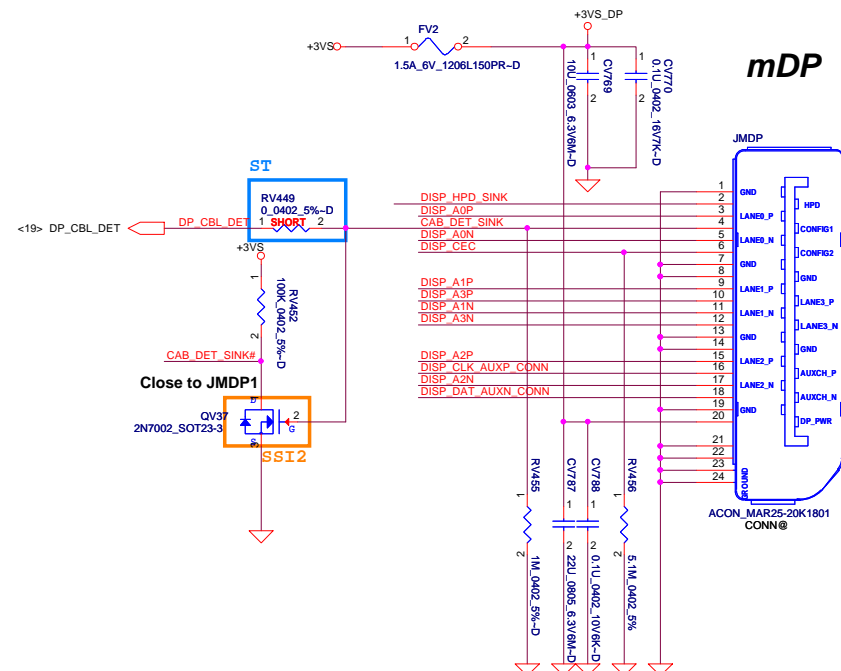
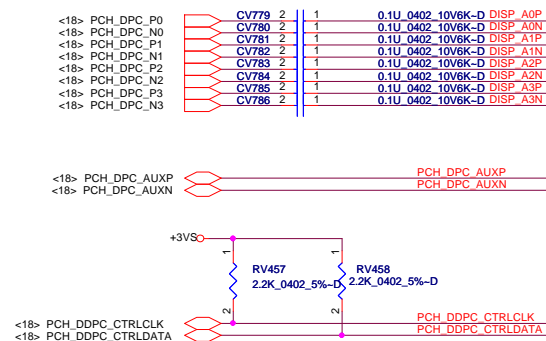


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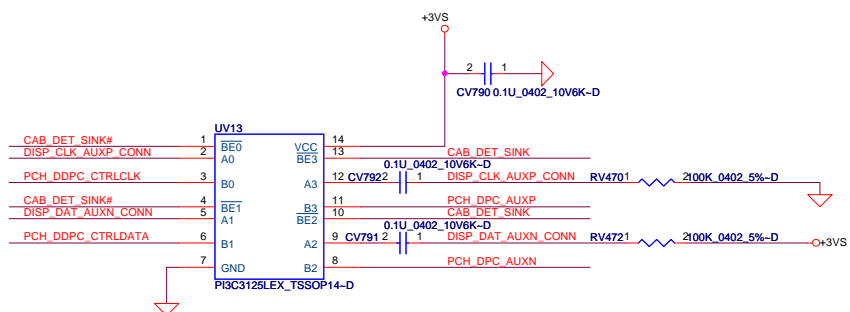


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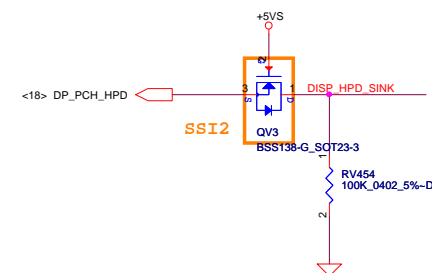
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				Custom	LA-7841P	Rev	0.3
				Date:	Tuesday, February 07, 2012	Sheet	36 of 65



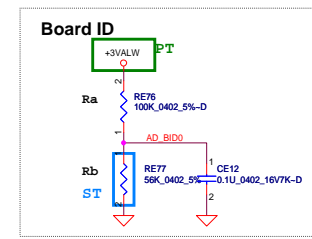
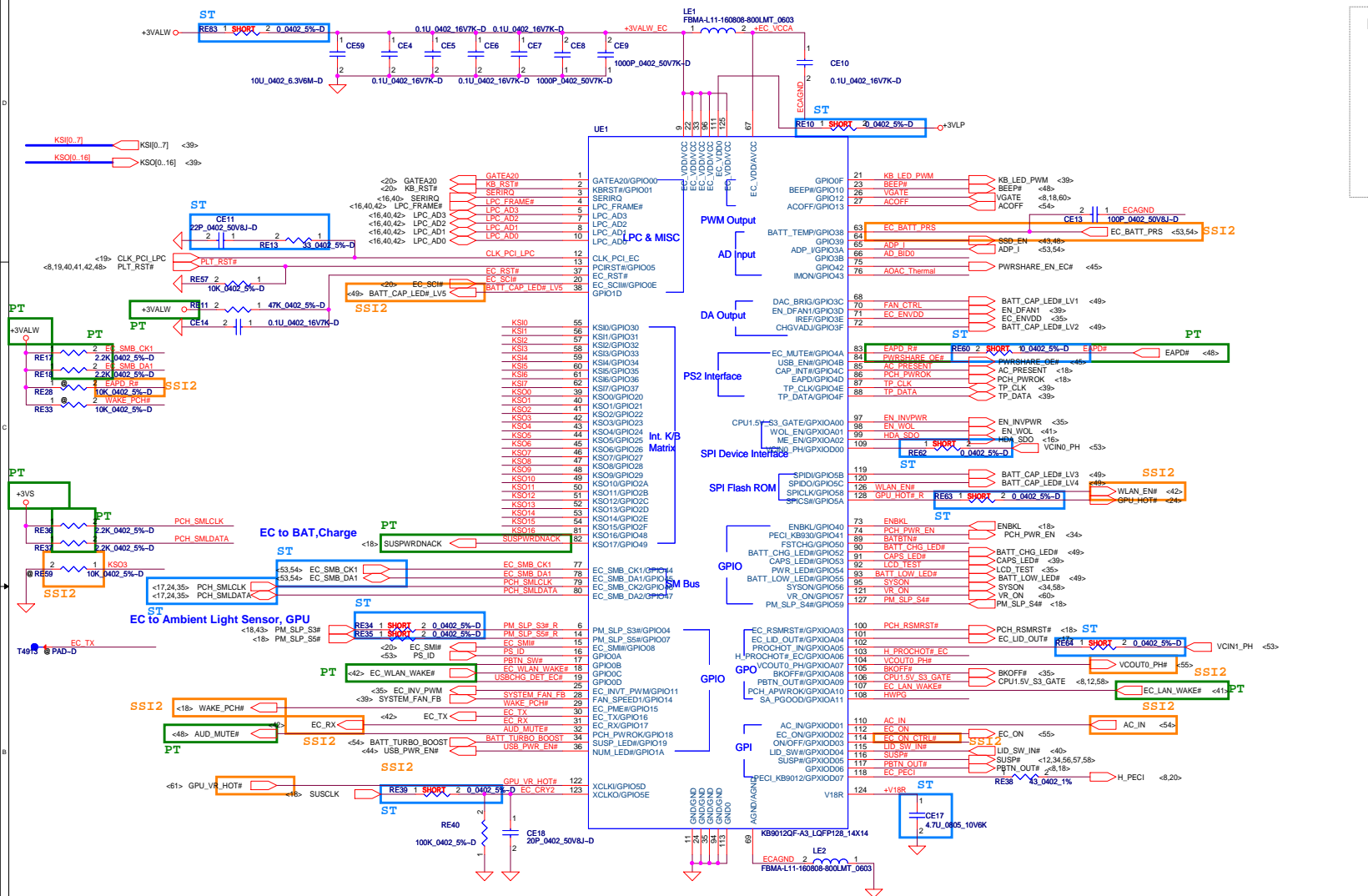
DDC Dongle SW for DP



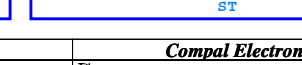
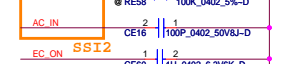
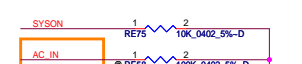
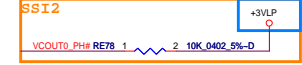
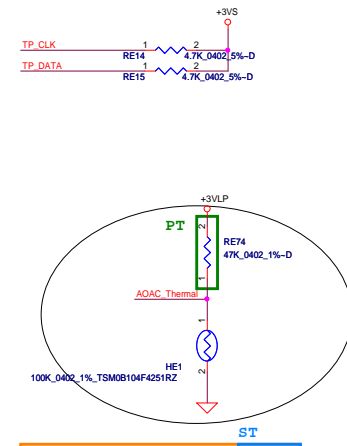
DP HPD to PCH (iGPU)



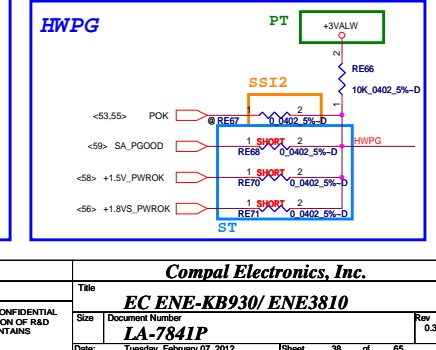
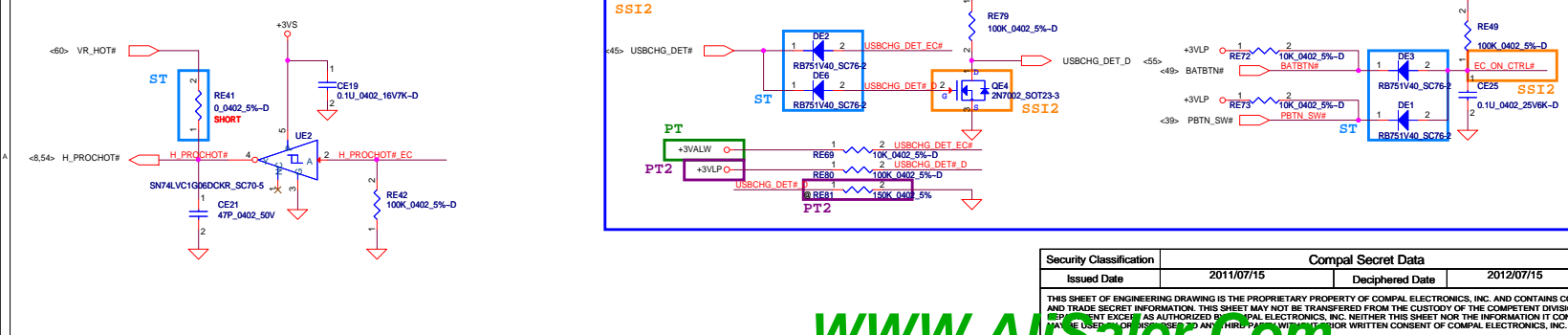
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Document Number LA-7841P				Date: Tuesday, February 07, 2012
Sheet 37 of 65				



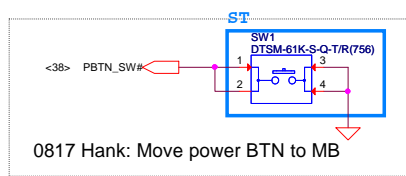
Page 4 for Board ID Rev. mapping



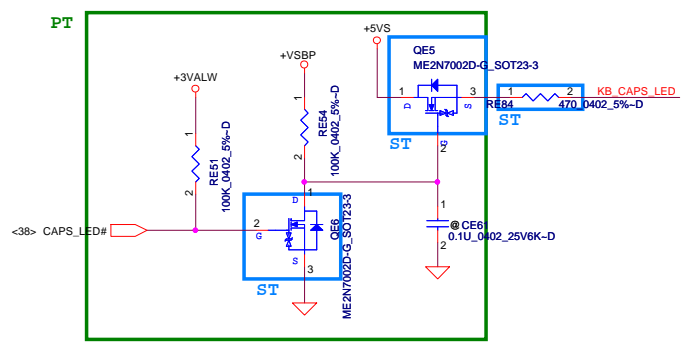
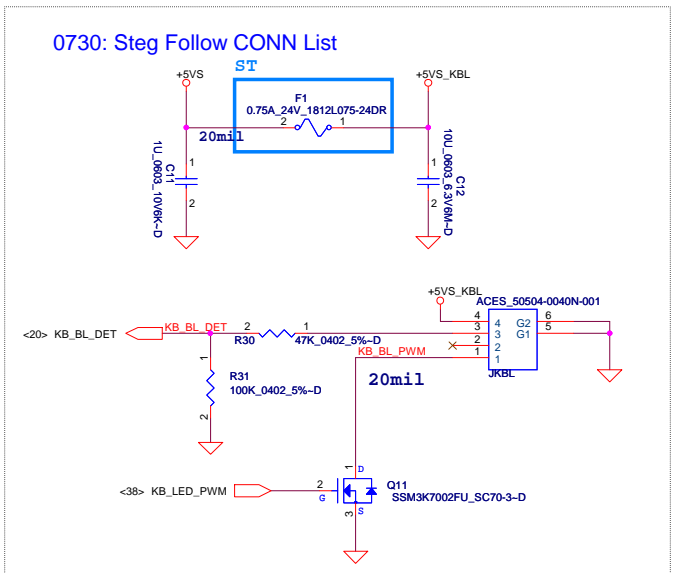
Power on Circuit



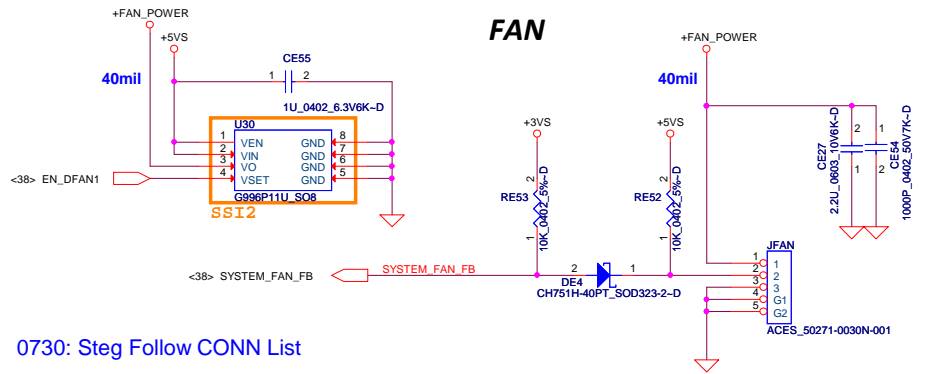
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Title	EC ENE-KB930/ ENE3810	
Size	Document Number	Rev
LA-7841P		0.3
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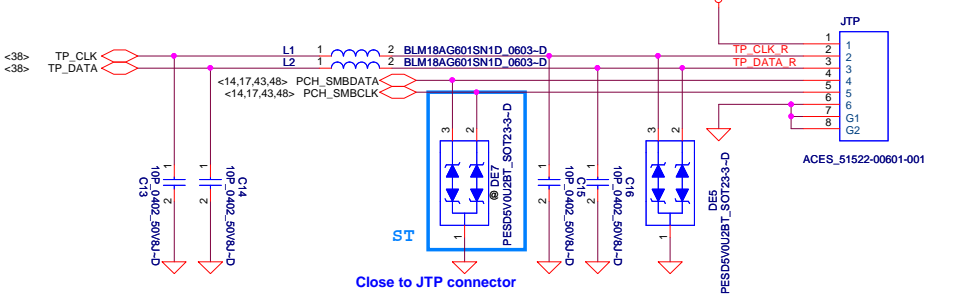
Keyboard back light



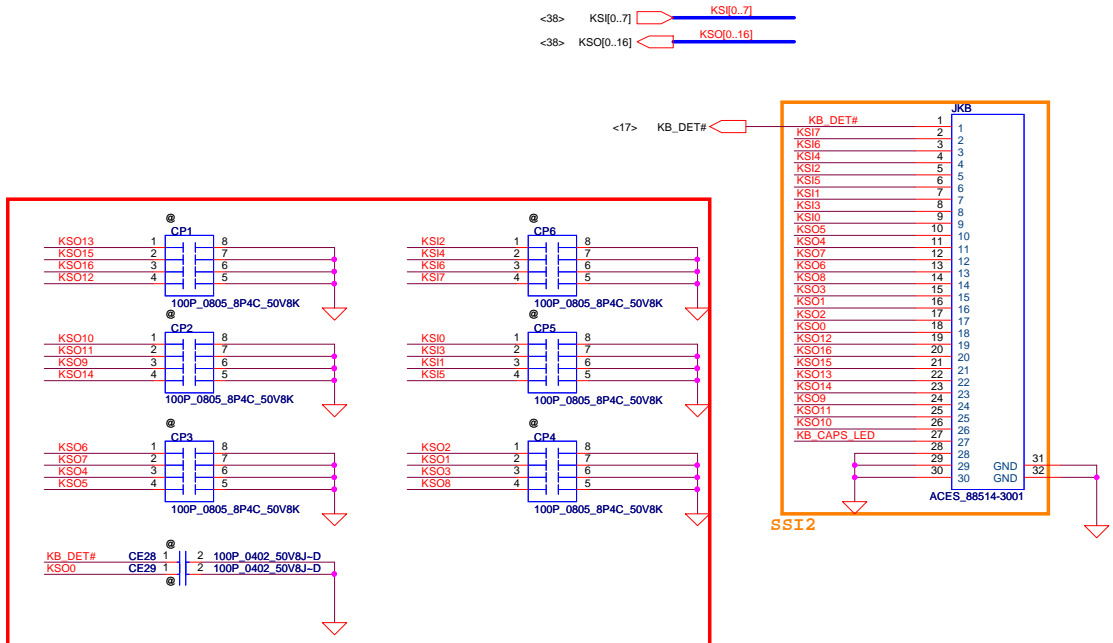
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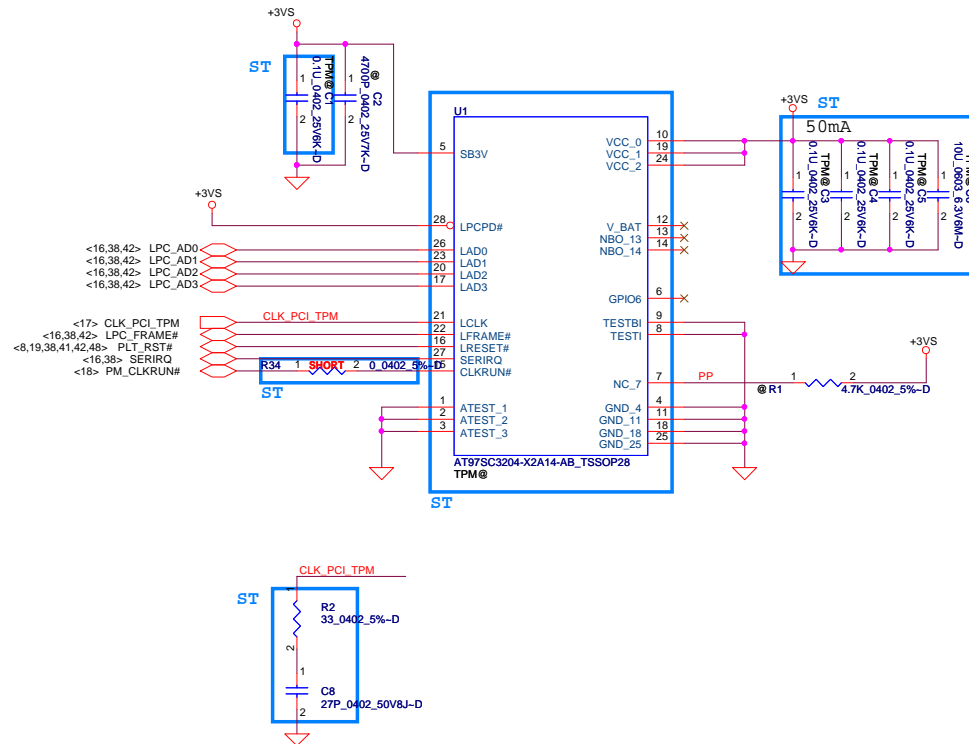
Touch pad



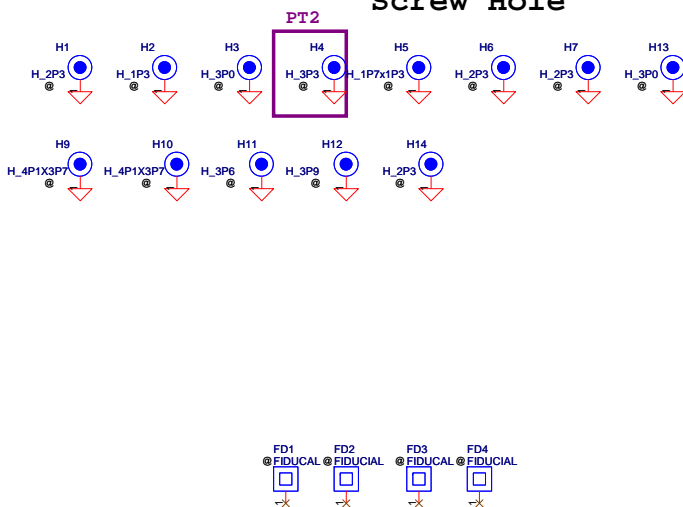
INT_KBD Conn.



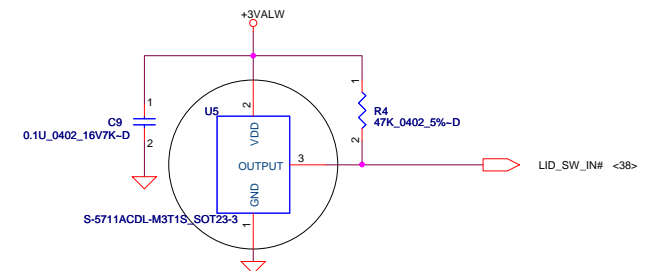
ATMEL TPM for XPS



Screw Hole

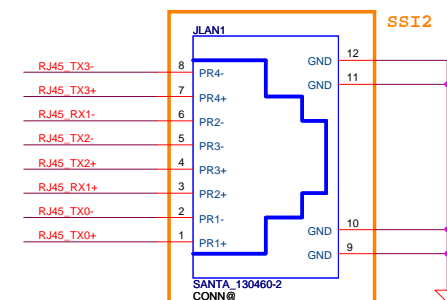
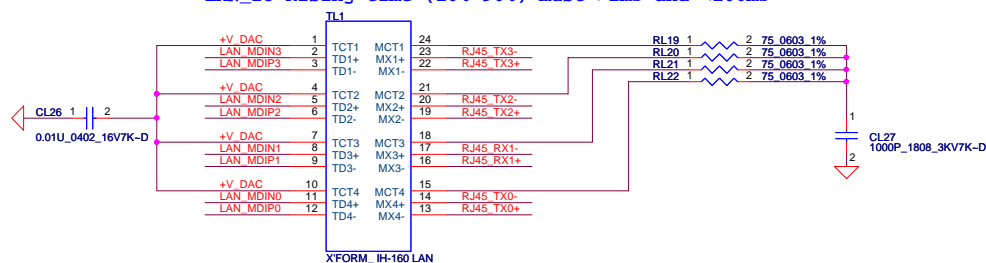
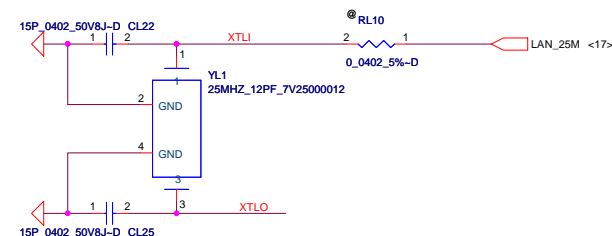
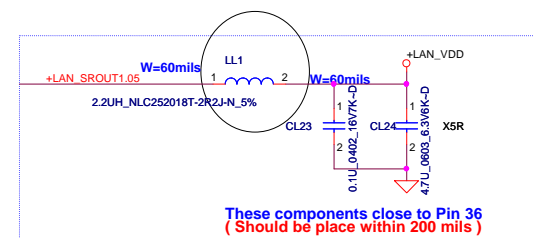
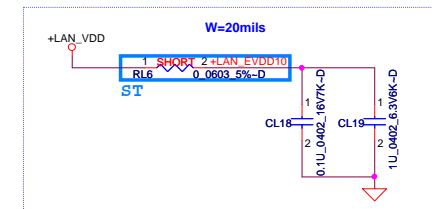


Lid Switch



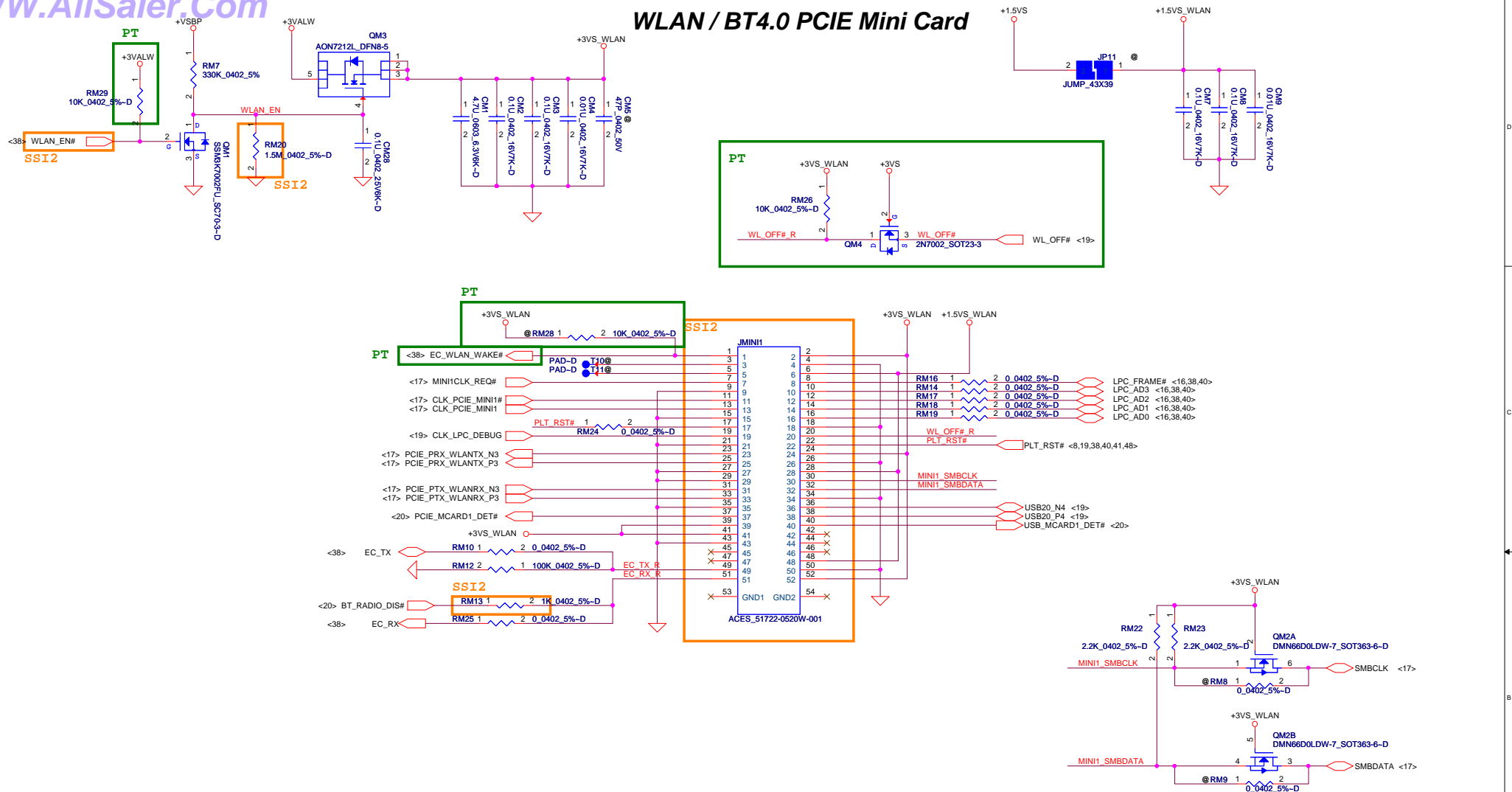
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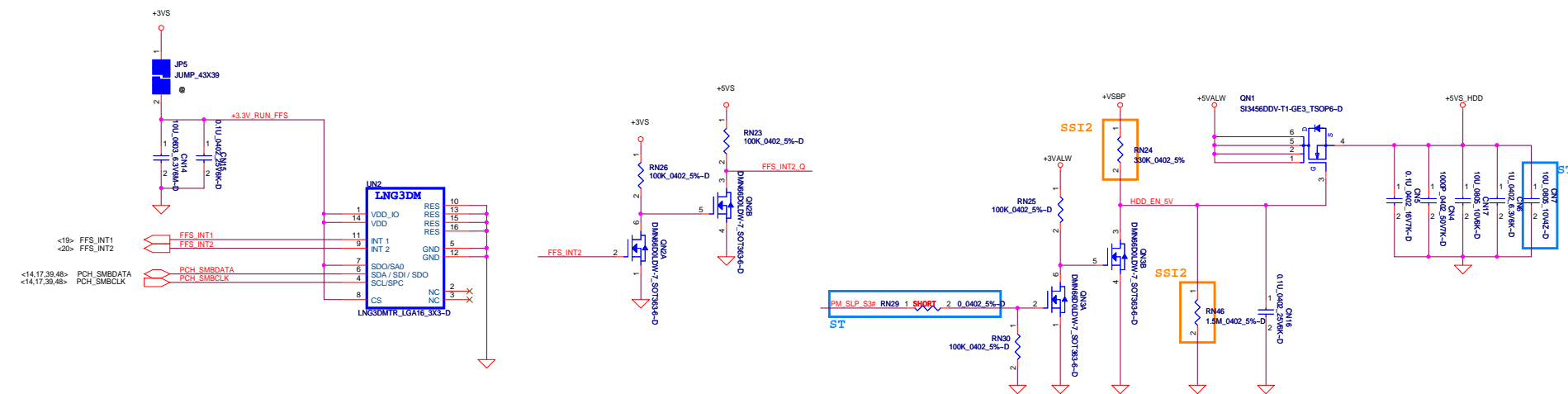
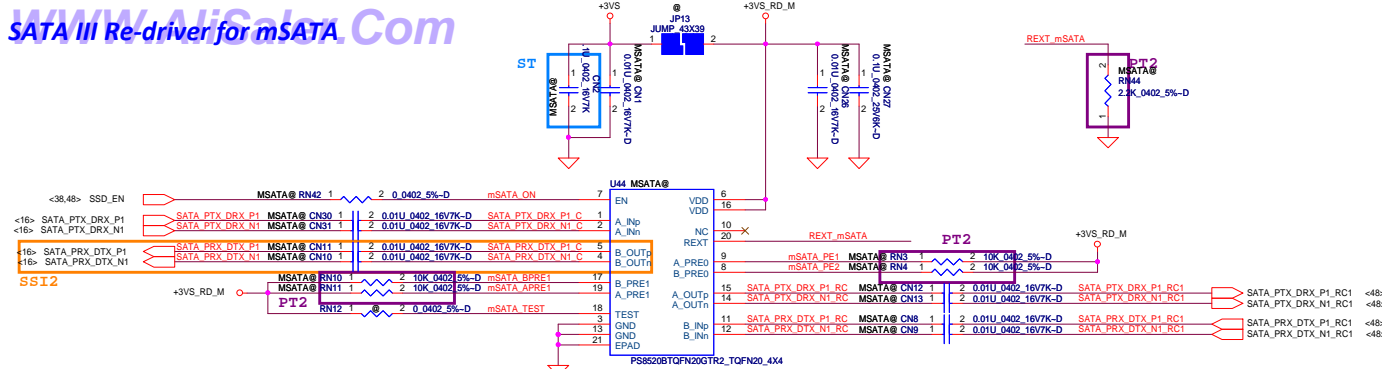
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								Rev 0.3			
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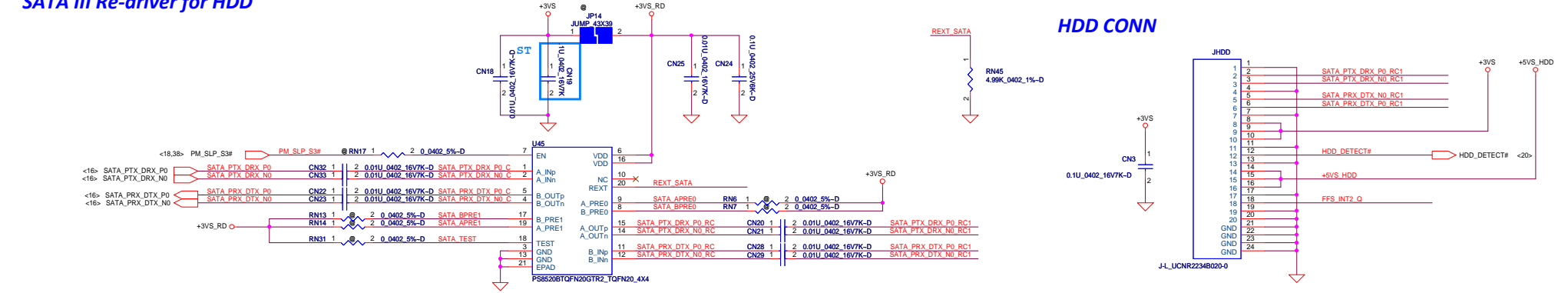
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WLAN / BT4.0 PCIE Mini Card



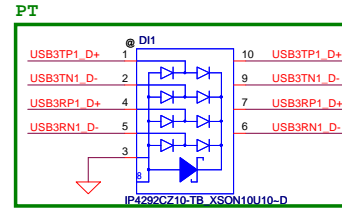
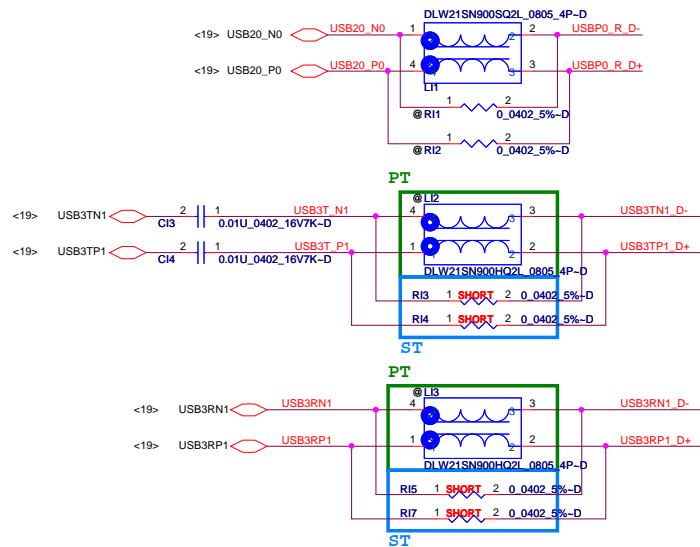


SATA III Re-driver for HDD

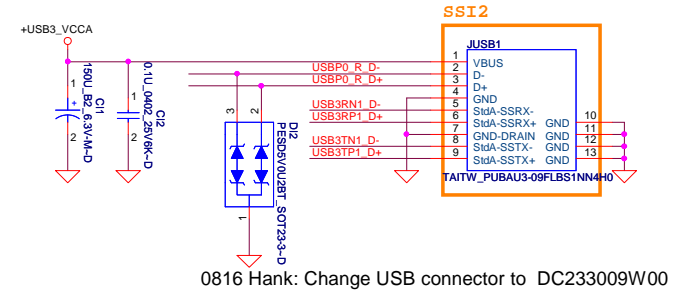


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Size	Document Number	LA-7841P	Rev	0.3
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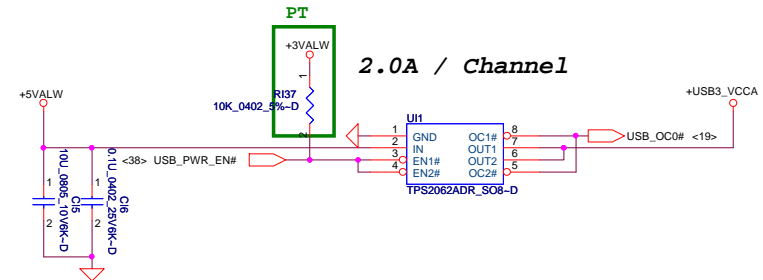
USB3.0 / USB2.0



Place close to JUSB1



2.0A / Channel



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				USB conn.			
				Document Number			
				LA-7841P			
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The schematic diagram illustrates the internal wiring of the USB20 module. Key components and connections include:

- Power Supply:** A +5VALW supply is connected to the module. It passes through a 100nF capacitor (C13) and a 10k resistor (R118) before reaching the USB20 chip (U12).
- USB20 Chip (U12):** The chip is a TP2062ADR_S08-D. Its pins are connected to the module's external pins:
 - Pin 1 (GND) to GND.
 - Pin 2 (IN) to +5VALW.
 - Pin 3 (EN1#) to PWRSHARE_EN#.
 - Pin 4 (EN2#) to USBP1_D+.
 - Pin 5 (OC2#) to USBP1_D-.
 - Pin 6 (OC1#) to SEL.
 - Pin 7 (OUT1) to SB#.
 - Pin 8 (OUT2) to INT#.
 - Pin 9 (GND) to GND.
- Resistors:**
 - R117 (10k) is connected between PWRSHARE_EN# and SB#.
 - R118 (10k) is connected between +5VALW and the IN pin of U12.
 - R119 (10k) is connected between +5VALW and the EN1# pin of U12.
 - R26 (10k) is connected between the EN2# pin of U12 and the SEL pin of U12.
- Capacitors:**
 - C11 (100nF) is connected between +5VALW and GND.
 - C12 (100nF) is connected between the IN pin of U12 and GND.
 - C13 (100nF) is connected between +5VALW and GND.
- Other Components:**
 - U13 (PT) is a power transistor used for switching the +5VALW supply to the USB20 chip.
 - U14 (SB#) is a Schmitt trigger buffer connected to the SB# pin of U12.
 - U15 (INT#) is a Schmitt trigger buffer connected to the INT# pin of U12.

USB3.0 / USB2.0



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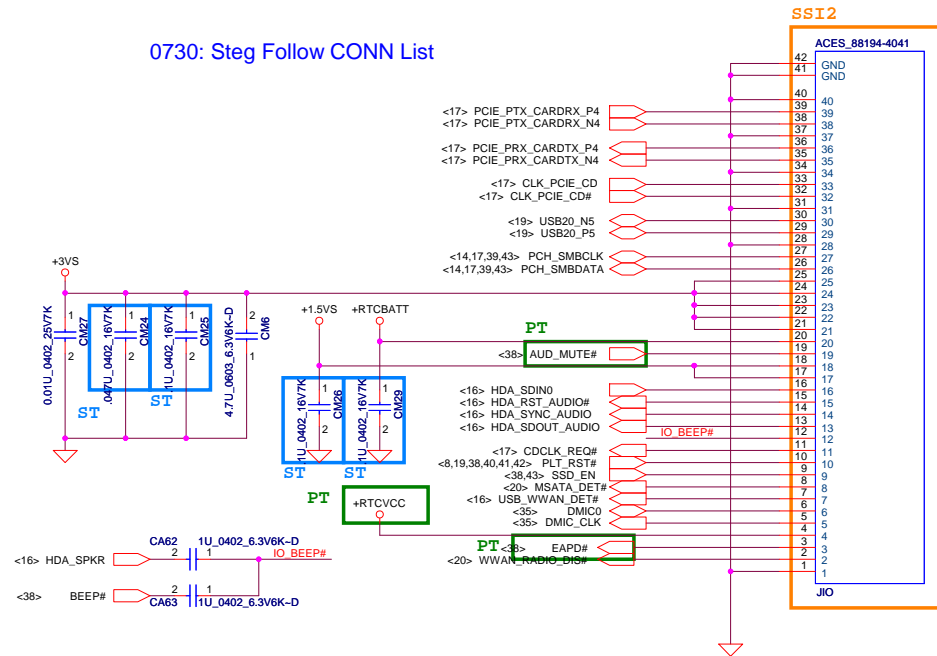
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WWW.AllSaler.Com

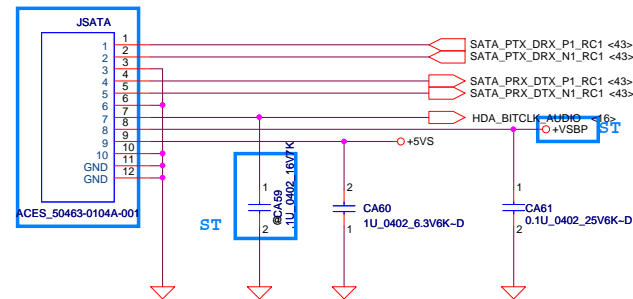
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				Custom	0.3
				Document Number	LA-7841P
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0730: Steg Follow CONN List

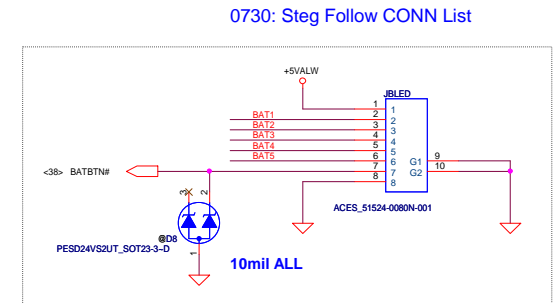
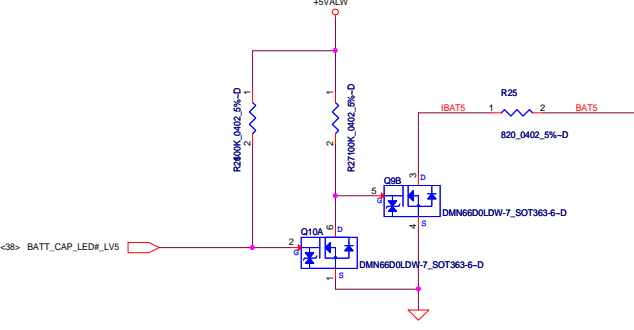
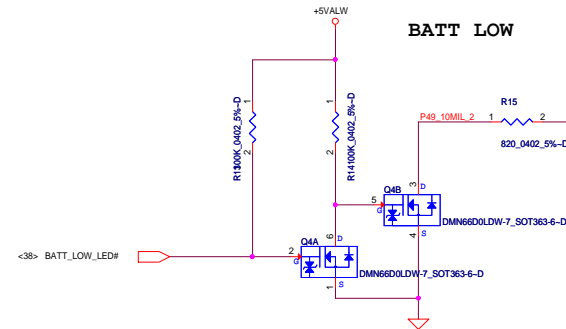
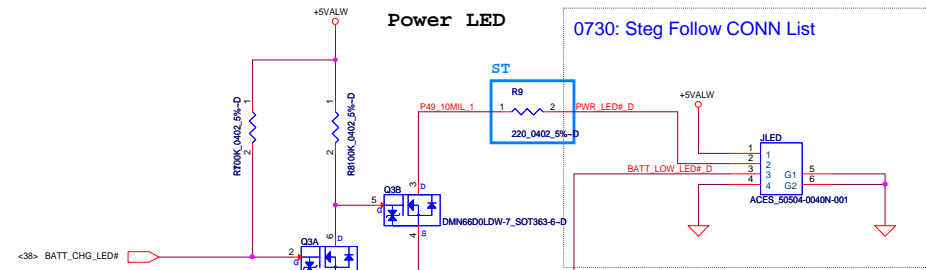
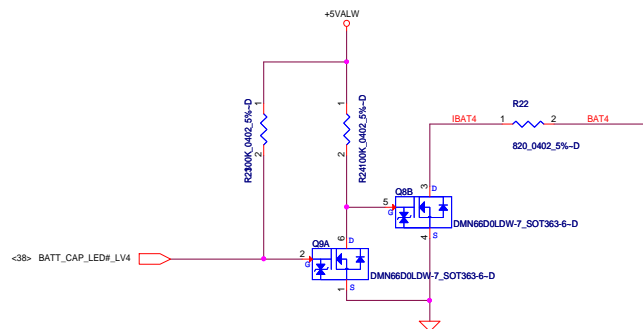
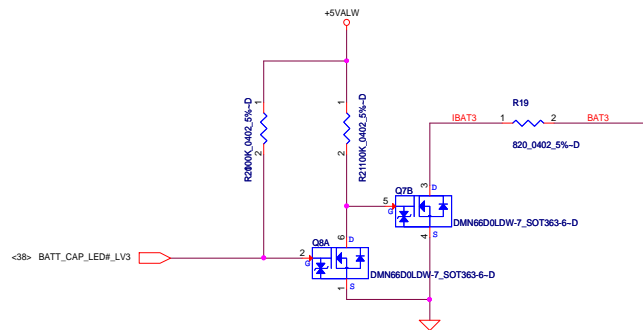
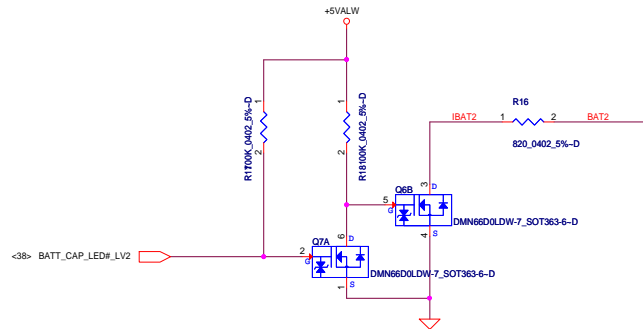
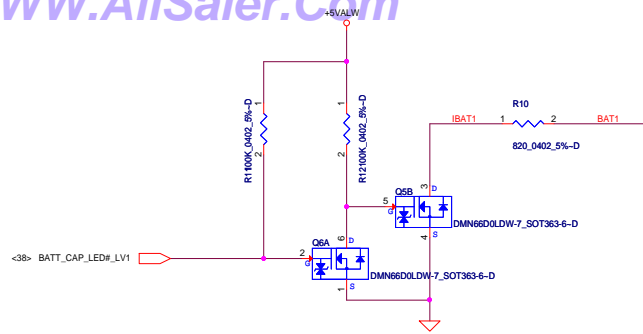


0805: Steg follow CIS Symbol



0816 Hank: P/N Correct, footprint Correct, but not CIS.

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Size	C	Document Number	LA-7841P	Rev
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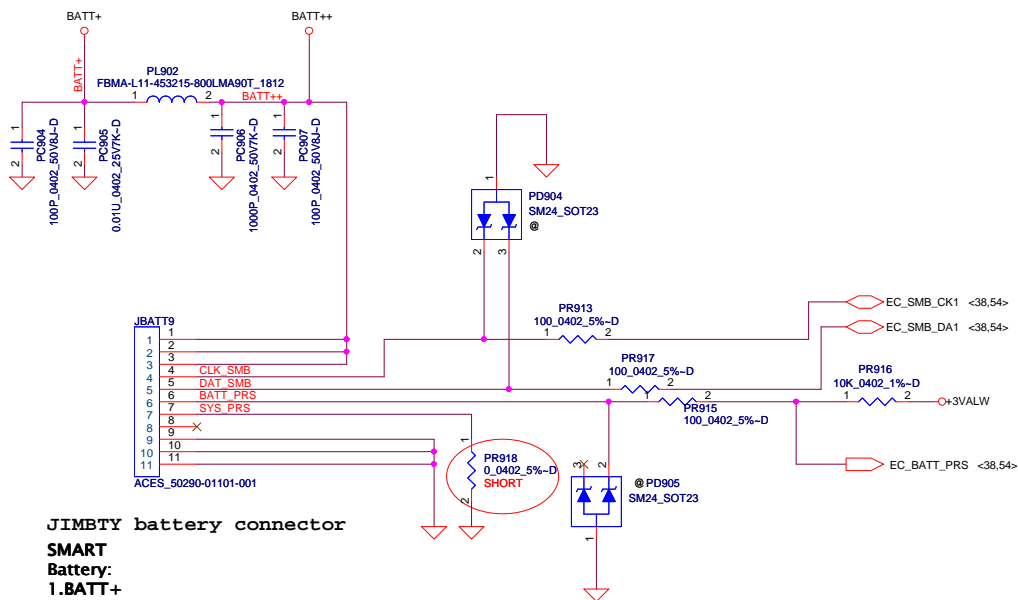
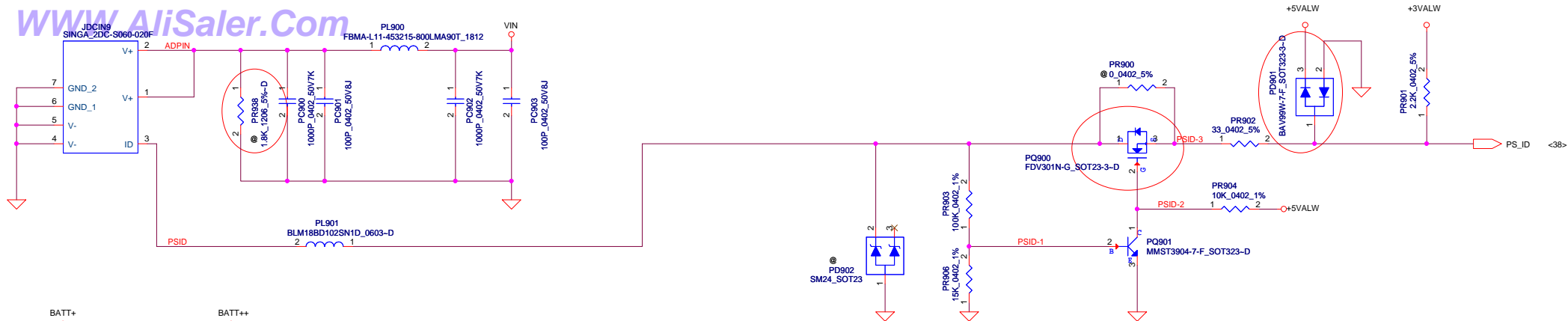
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3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

	5	4	3	2	1
D					
C					
B					
A					

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SizeA	Document Number<Doc>			Rev0.3
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D					
C					
B					
A					

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JIMBTY battery connector

SMART

Battery:

1.BATT+

2.BATT+

3.BATT+

4.CLK_SMB

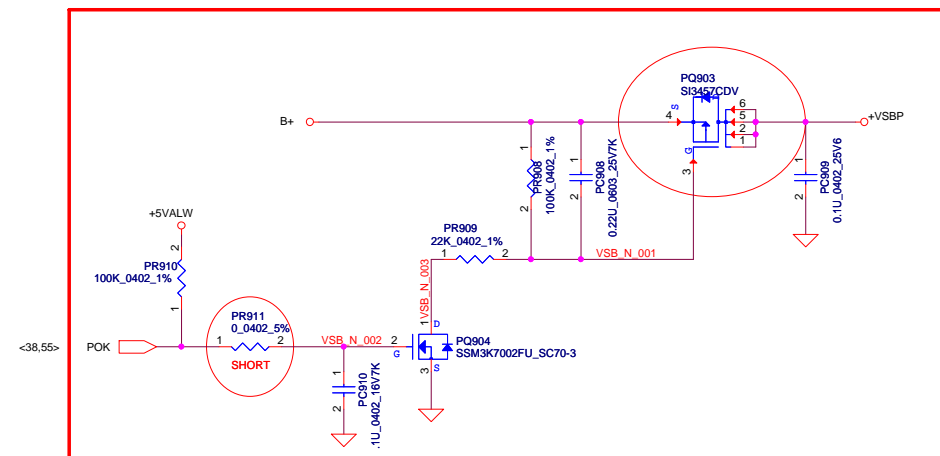
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6.BATT_PRS

7.SYS_PRES
8.DAT_ALERT

8.BAT_A
9.CND

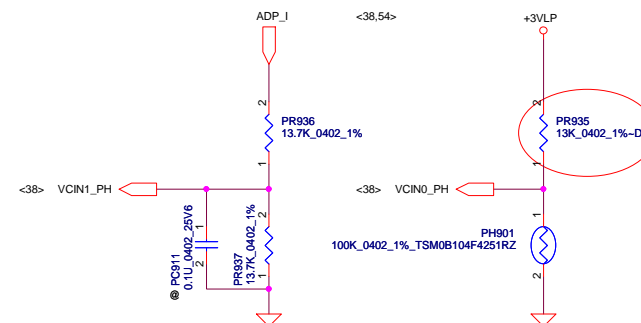
9.GND
10.GND

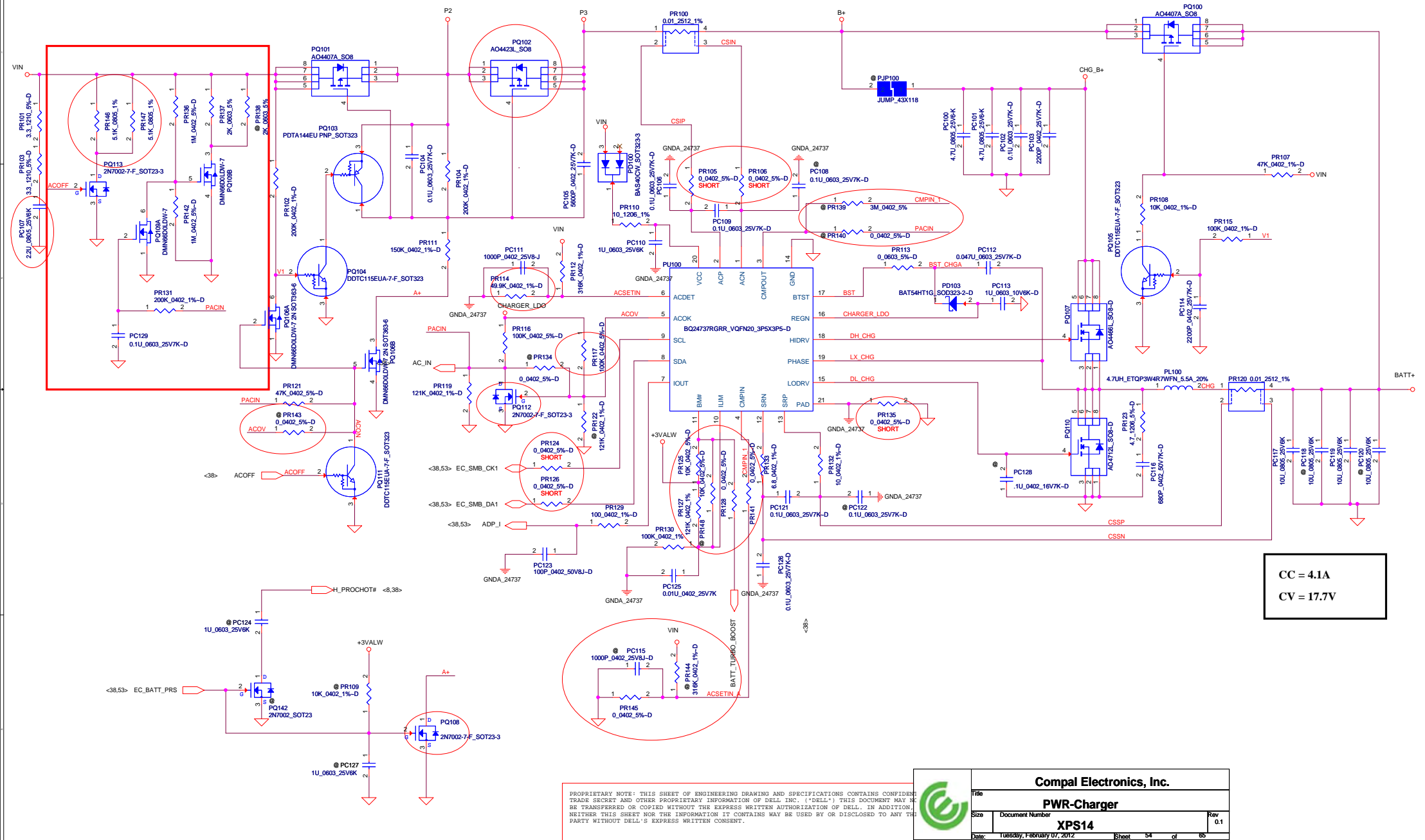
10.GND
11.GND

PH901 under CPU botten side :

CPU thermal protection at 90 degree C

Recovery at 50 degree C



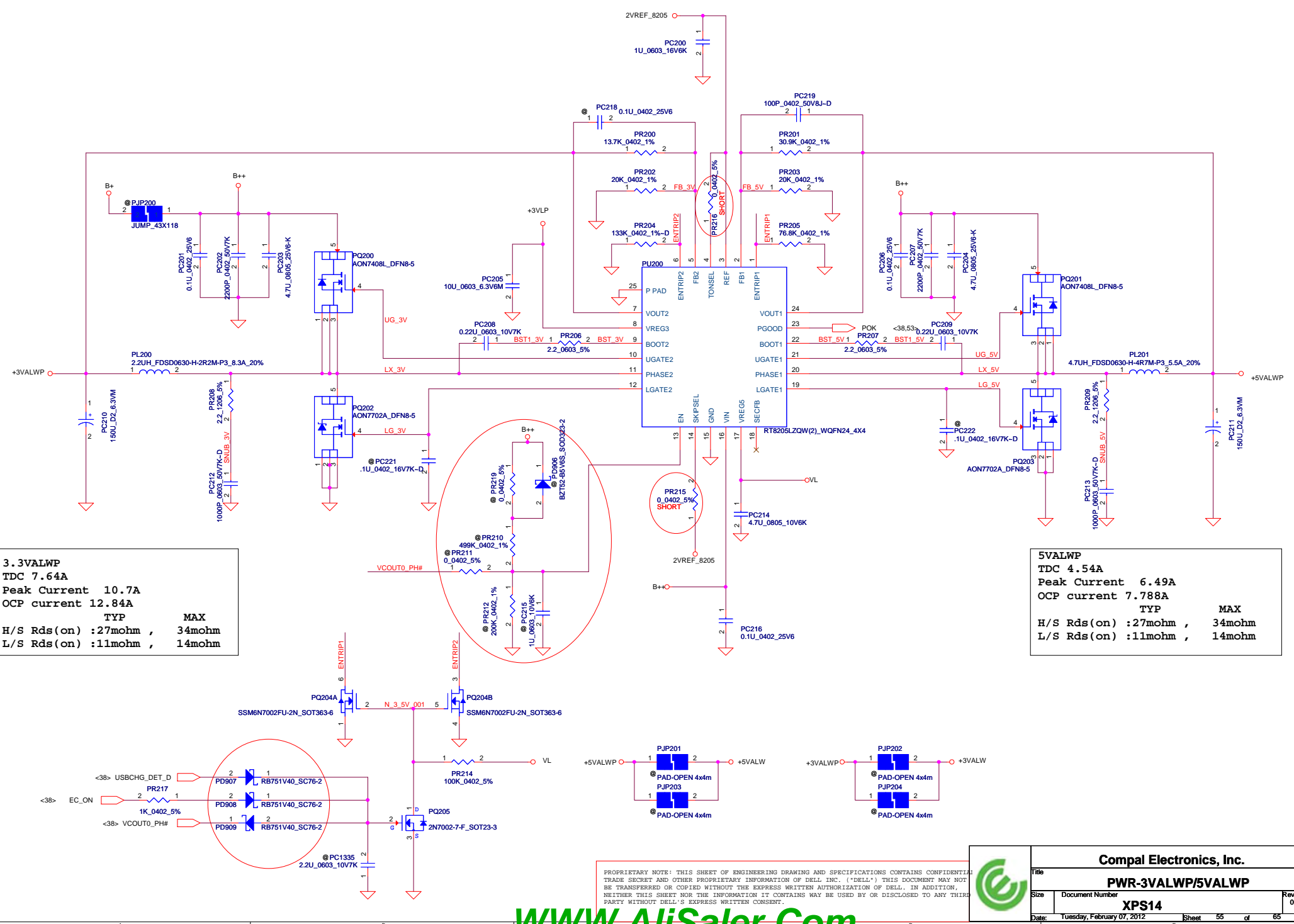


3.3VALWP
TDC 7.64A
Peak Current 10.7A
OCP current 12.84A

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H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:11mohm	14mohm

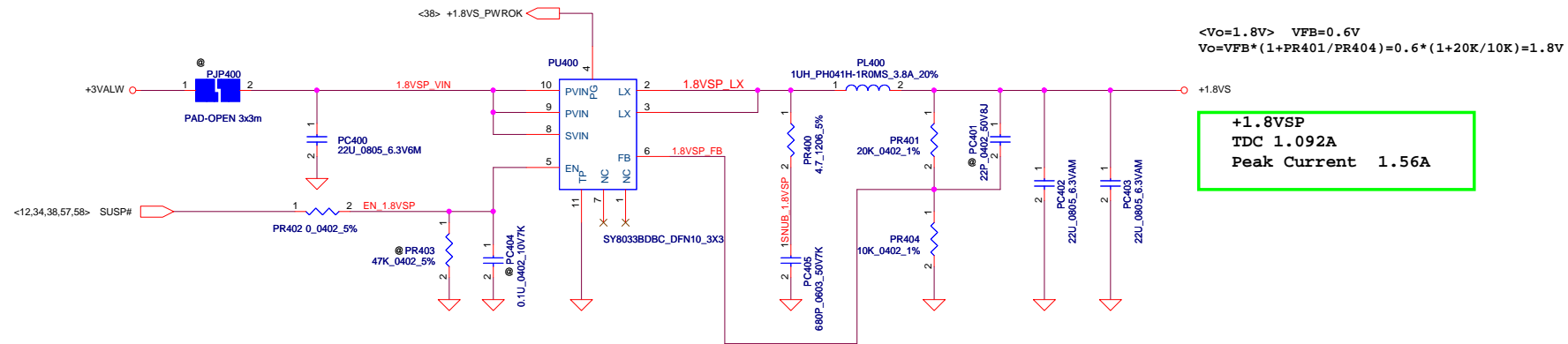
5VALWP
TDC 4.54A
Peak Current 6.49A
OCP current 7.788A

	TYP	MAX
H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:11mohm	14mohm

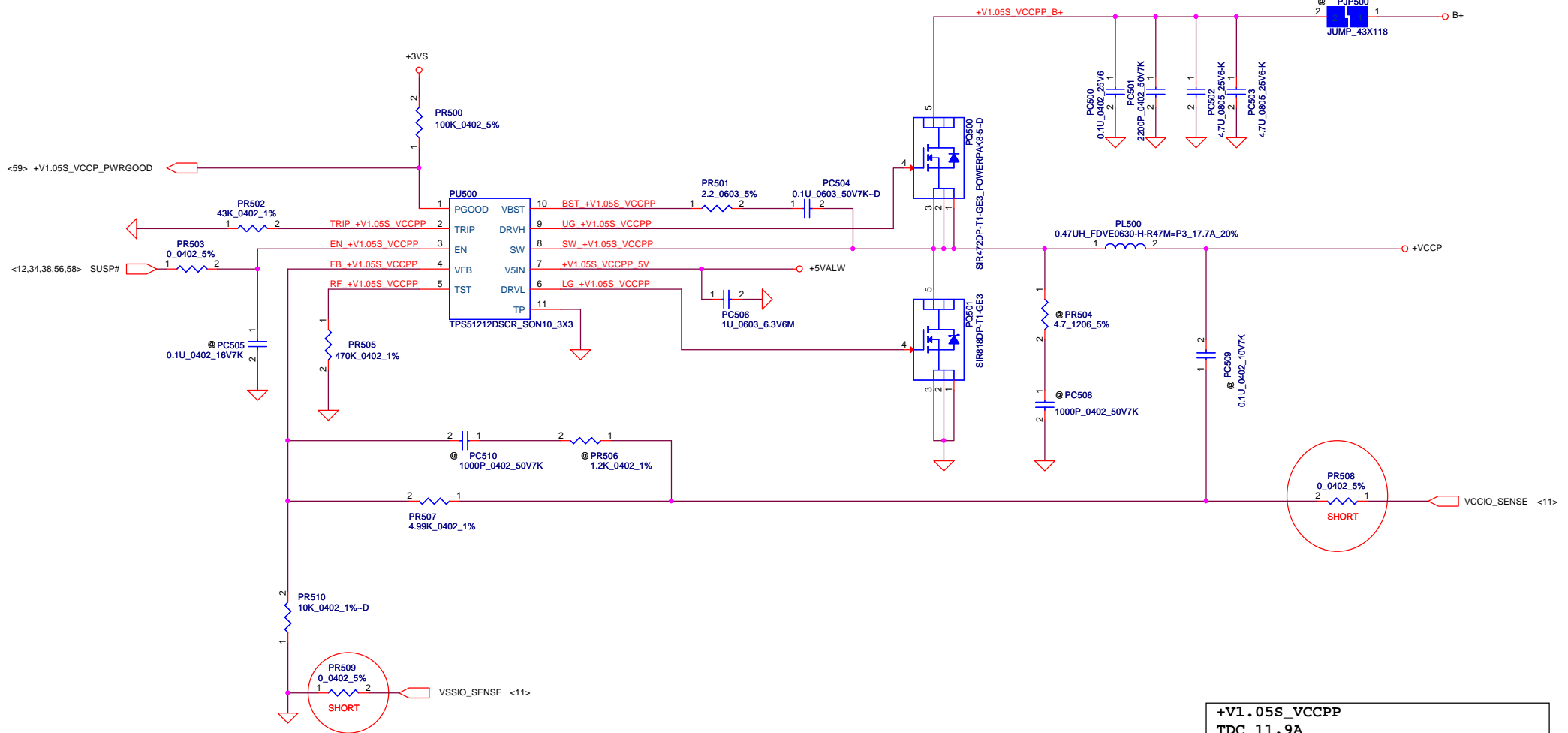


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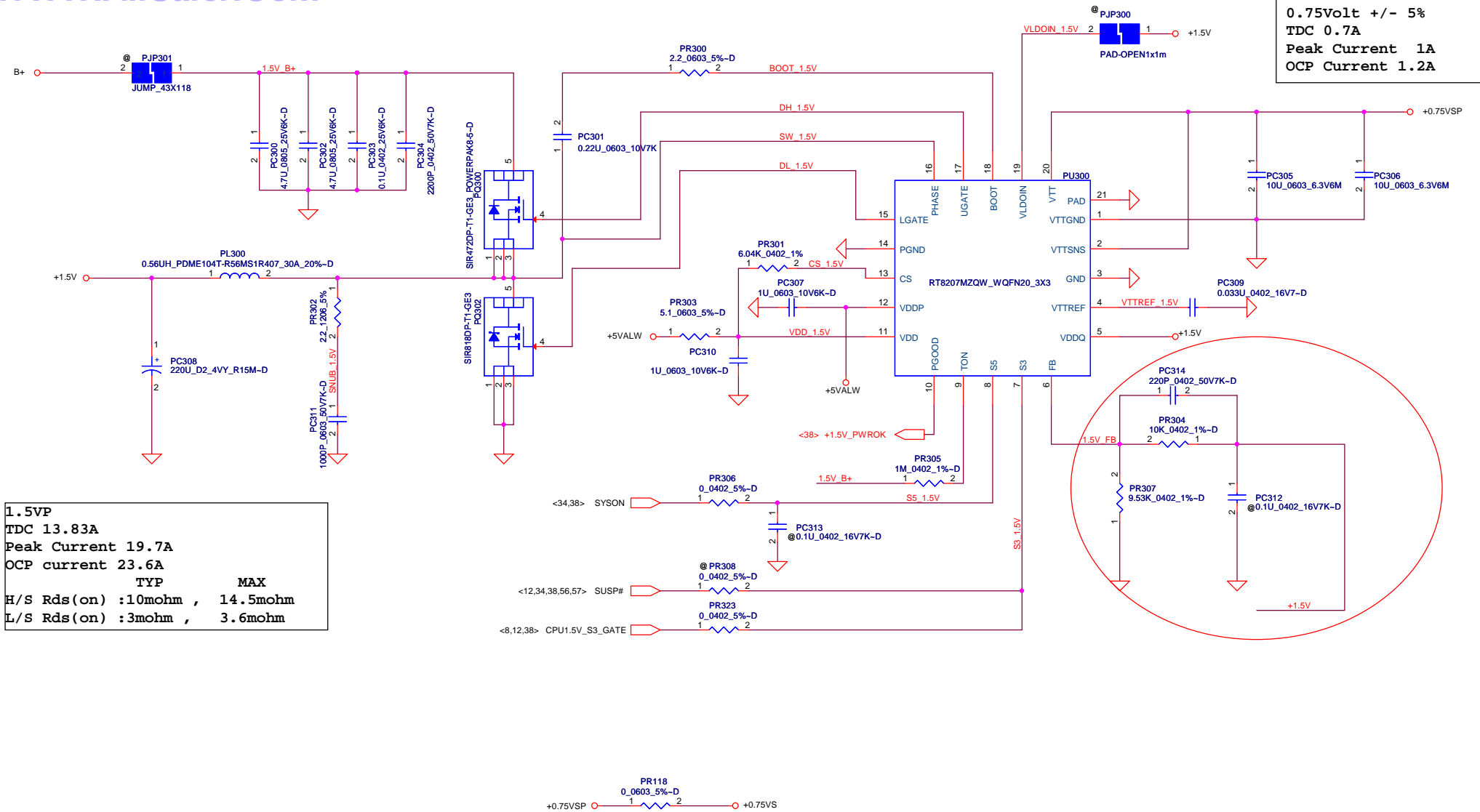
+V1.05S_VCCPP	
TDC 11.9A	
Peak Current 17A	
OCP current 20.4A	
	TYP MAX
H/S Rds(on) :	10mohm , 14.5mohm
L/S Rds(on) :	3mohm , 3.6mohm

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1.5VP
TDC 13.83A
Peak Current 19.7A
OCP current 23.6A

	TYP	MAX
H/S Rds(on)	:10mohm	14.5mohm
L/S Rds(on)	:3mohm	3.6mohm

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

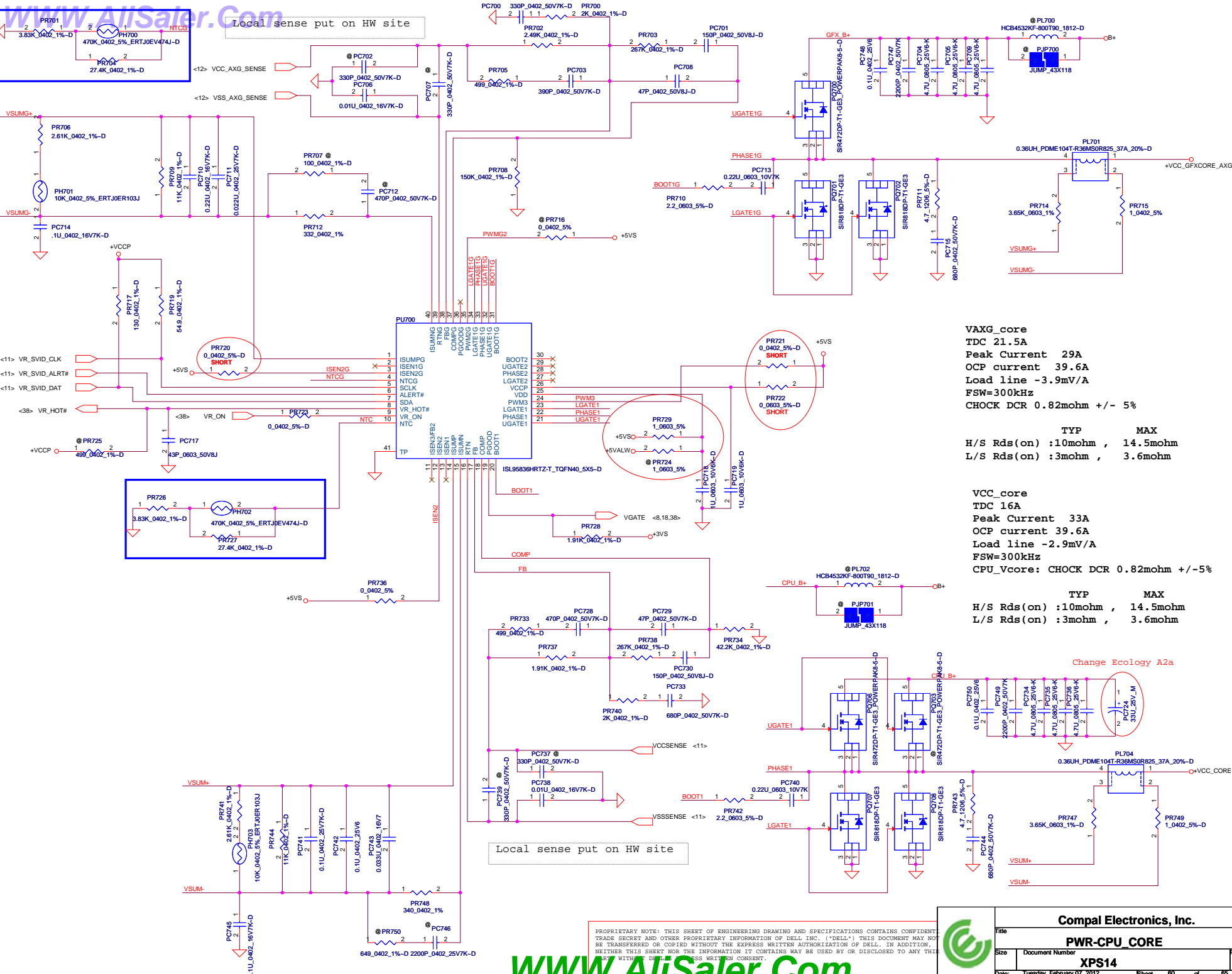
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Title		PWR-1.5VP/0.75VSP	
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Compal Electronics, Inc.

XPS14

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VAXG_core
TDC 21.5A
Peak Current 29A
OCP current 39.6A
Load line -3.9mV/A
FSW=300kHz
CHOCK DCR 0.82mohm +/- 5%


TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm

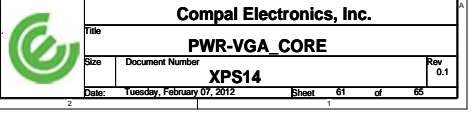
VCC_core
TDC 16A
Peak Current 33A
OCP current 39.6A
Load line -2.9mV/A
FSW=300kHz
CPU_Vcore: CHOCK DCR 0.82mohm +/-5%

TYP MAX
H/S Rds(on) :10mohm , 14.5mohm
L/S Rds(on) :3mohm , 3.6mohm

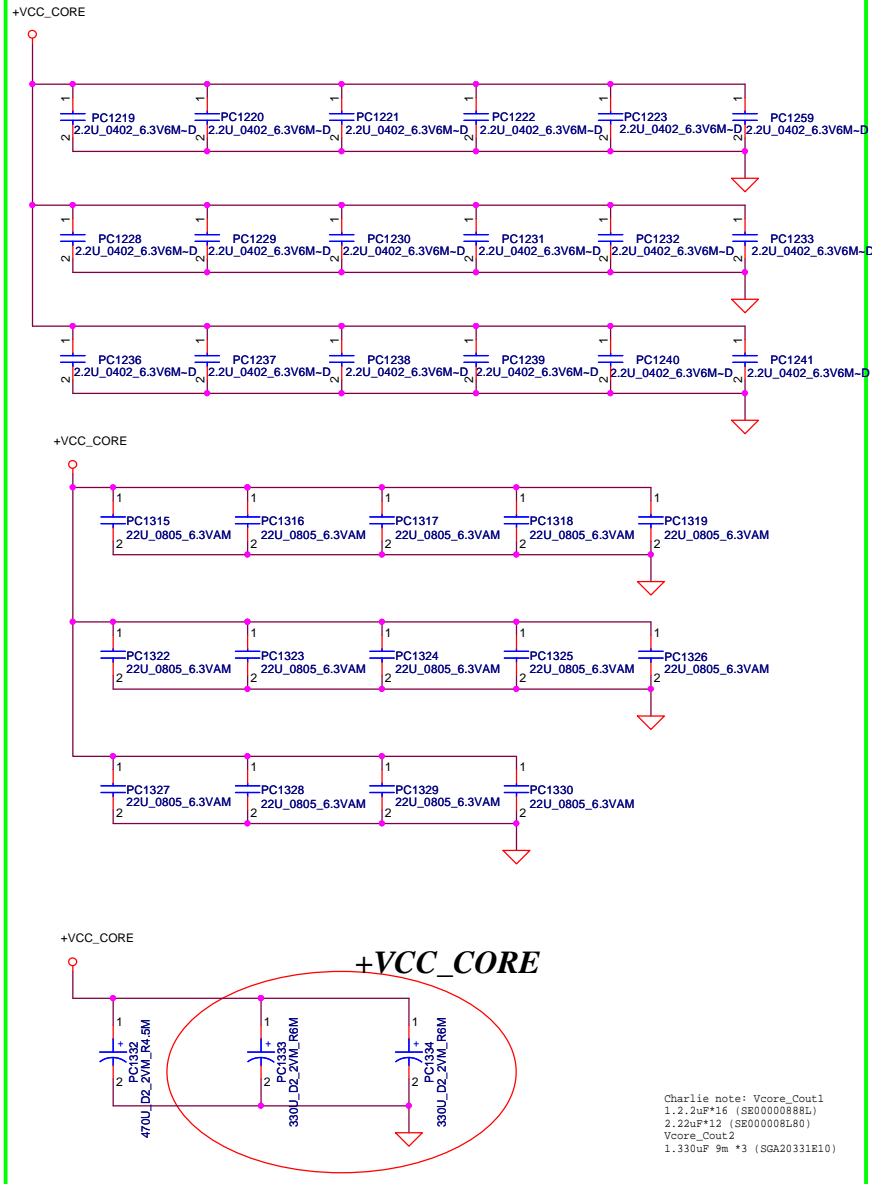
Change Ecology A2a

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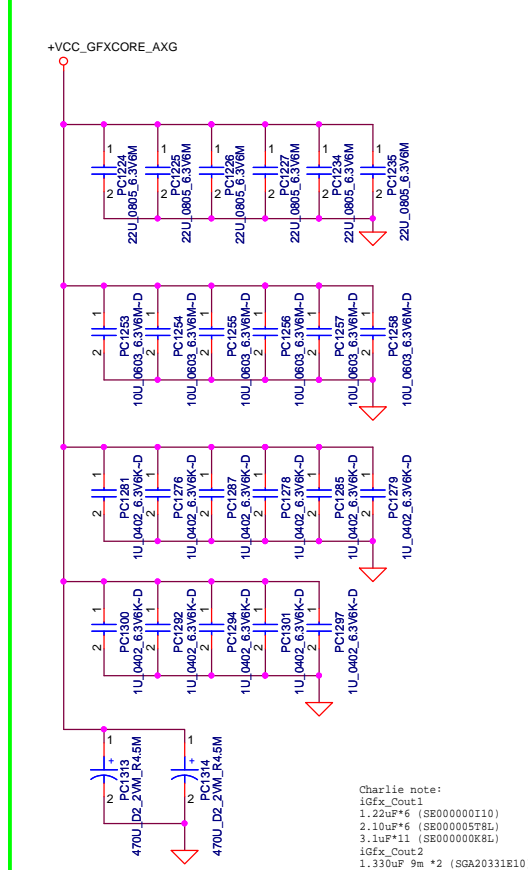
	Compal Electronics, Inc.			
	Title PWR-CPU_CORE			
	Size	Document Number XPS14		Rev 0.1
	Date: Tuesday, February 07, 2012	Sheet 60	of 65	



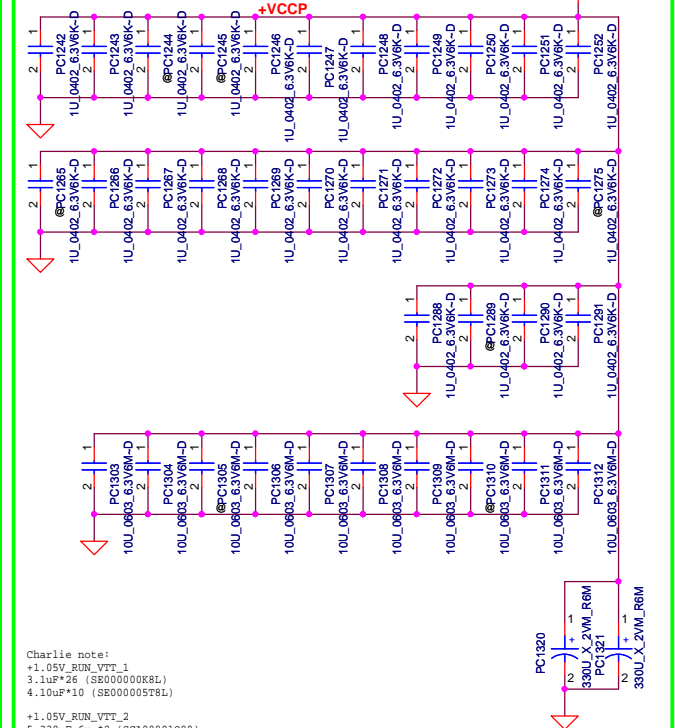
+VCC_CORE



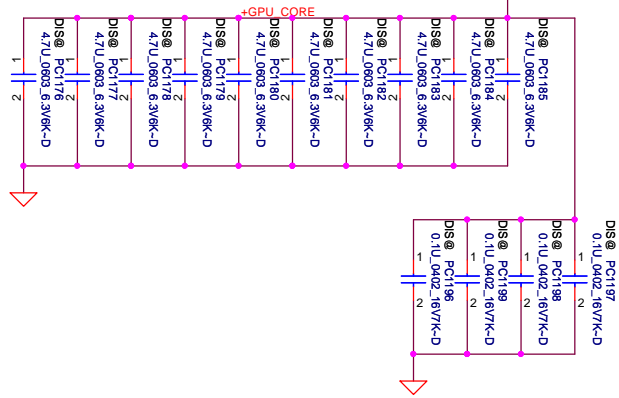
+VCC GFXCORE_AXG



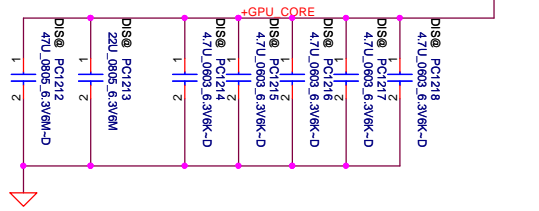
+VCCP



+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



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Title		GPU DECOUPLING	
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Title			
PWR-PIR			
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description			Solution Description																																																																																		
QLM00	1	38	01/12			1.0	PCB REV change to 1.0			Change RE77 to 56K																																																																																		
	2	24	01/12			1.0	Change EC_SMB_CK2_PX/EC_SMB_DA2_PX pull up resistor as design guide			Change RV2420,RV2421 to 2.2K																																																																																		
	3	39	01/12			1.0	Adjust CAPS_LED brightness			Change RE84 to 470ohm																																																																																		
	4	45	01/12			1.0	Sync up with XPS 15" for pull up power rail			RI38 pull up from +5VALW to +3VALW																																																																																		
	5	17,24,35	01/12			1.0	Solve adaptor detect issue			Depop QH3; change GPU SMBus/Ambient Light Sensor connect to PCH_SMLDATA and PCH_SMLCLK																																																																																		
	6	45	01/12			1.0	Purchase recommend			Change UI3 to high active parts																																																																																		
	7	40	01/12			1.0	BOM structure control			ADD TPM@ for TPM circuit																																																																																		
	8	38	01/12			1.0	For USBCHG_DET_D can't turn on 3V/5V issue			Change RE78 pull up to +3VLP																																																																																		
	9	45	01/12			1.0	Vendor recommend			UI2 EN pin pull up resistor RI38 change to 10K																																																																																		
	10	35	01/12			1.0	Change JLVDS connector PN and footprint as assembly issue			Change JLVDS connector PN to SP01001BT00, footprint to ACES_59003-04006-001_40P																																																																																		
	11	39	01/12			1.0	ME change			SW1 PN change to SN100005100																																																																																		
	12	33	01/16			1.0	Solve 1.5V voltage drop issue			Change QV2803 to SB00000SJ0L to lower Rds on																																																																																		
	13		01/16			1.0	Remove 0 ohm to short pad for MP			RI22,RI23,RI24,RI25,RI17,RI3,RI4,RI5,RI7,RN29,RM10,RM25,RL25,RL6,R34,RE83, RE10,RE34,RE35,RE39, RE68,RE70,RE71,RE60,RE62,RE63,RE64,RV449, RV3519,RV3517,RI6,RI8,RV3525,RH199,RH105,RH106,RH108,RH110,RH112,RH101, RH103,RH107,RH44,RU125,RU122,RU123,RU116,RU131,RU75,RU62																																																																																		
	14	10	01/17			1.0	Change setting for Ivy Bridge support 1x16 PCI Epress and Sandy Bridge only UMA Config			Depop RU85																																																																																		
	15	49	01/17			1.0	ME requirement for LED brightness tuning			R9 Change to 220ohm for Power LED(White)																																																																																		
	16	39	01/18			1.0	EMI requirement			Add DE7 on TP SMBus																																																																																		
	17	38,35,39	01/19			1.0	Thailand flood disaster, original material shortage			Change DE1,DE2,DE3,DE6 PN to SCS00002G00; QE5,QE6,QV3508,QZ10,QZ13,QZ15 to SB00000M700; DV9 to SCS00002G00																																																																																		
	18	35	01/19			1.0	JLVDS pin define change for opertion risk			JLVDS Pin38 NC and up shift to Pin33																																																																																		
	19	33	01/20			1.0	Change HF part			Change RZ10,RZ11,RZ40,RZ41 PN to SD028220A8L																																																																																		
	20	48	01/20			1.0	Manufacture highlight change			Change JSATA footprint to ACES_50463-0104A-001_10P-T																																																																																		
	21	17,19,40	01/20			1.0	EMI requirement			Populate PCI CLK reserved parts RH65,CH26,CH31,R2,C8																																																																																		
	22	36	01/20			1.0	EMI requirement for LVDS			Change LV7,LV8,LV9,LV10 to SM070002S00																																																																																		
	23	39	01/30			1.0	Change HF part			Change F1 to SP040003200																																																																																		
	24	48,53	01/30			1.0	Solve audio power consumption issue			Change PQ903 PN to SB93457001L, JSATA pin8 B+ change to +VSBP																																																																																		
	25	17,38	01/30			1.0	EMI requirement			Populate CH98,CE11,RE13																																																																																		
	26	14	02/01			1.0	1.5V power rail reach up to 1.614V, change for derating concern			CD7 capacitor change from 2V to 2.5V																																																																																		
	27	15	02/02			1.0	EMI requirement			Add RV3529,RV3530,CV3528,CV3529																																																																																		
	28		02/02			1.0	Customer concern Y5V MLCC performance			Change CA59 to SE076104K80; CE17 to SE064475KL0;CN2,CH11,CN19,CM25,CM26, CM29,CU33,CU34,CU35,CU36,CU97,CU155 to SE076104K80; CM24,CU39 change to SE076473K80; CN7,CZ11,CV3508 change to SE064106M8L																																																																																		
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<table><tr><td colspan="2">Security Classification</td><td colspan="4">Compal Secret Data</td><td colspan="7">Compal Electronics, Inc.</td></tr><tr><td colspan="2">Issued Date</td><td colspan="2">2011/07/15</td><td colspan="2">Deciphered Date</td><td colspan="2">2012/07/15</td><td colspan="5">Title</td><td></td></tr><tr><td colspan="8" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE REPRODUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td colspan="5">Change List</td><td></td></tr><tr><td>Size</td><td colspan="4">Document Number</td><td colspan="5">Rev</td></tr><tr><td colspan="8"></td><td colspan="5">LA-7841P</td><td>0.3</td></tr><tr><td colspan="8">Date:</td><td colspan="2">Tuesday, February 07, 2012</td><td colspan="2">Sheet</td><td>65</td><td>of</td><td>65</td></tr></table>													Security Classification		Compal Secret Data				Compal Electronics, Inc.							Issued Date		2011/07/15		Deciphered Date		2012/07/15		Title						THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE REPRODUCED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Change List						Size	Document Number				Rev													LA-7841P					0.3	Date:								Tuesday, February 07, 2012		Sheet		65	of	65
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